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Neuromorphic Engineering: From Biological to Spike-Based Hardware Nervous Systems

Jia-Qin Yang, Ruopeng Wang, Yi Ren, Jing-Yu Mao, Zhan-Peng Wang, Ye Zhou, and Su-Ting Han**

The human brain is a sophisticated, high-performance biocomputer that processes multiple complex tasks in parallel with high efficiency and remarkably low power consumption. Scientists have long been pursuing an artificial intelligence (AI) that can rival the human brain. Spiking neural networks based on neuromorphic computing platforms simulate the architecture and information processing of the intelligent brain, providing new insights for building AIs. The rapid development of materials engineering, device physics, chip integration, and neuroscience has led to exciting progress in neuromorphic computing with the goal of overcoming the von Neumann bottleneck. Herein, fundamental knowledge related to the structures and working principles of neurons and synapses of the biological nervous system is reviewed. An overview is then provided on the development of neuromorphic hardware systems, from artificial synapses and neurons to spike-based neuromorphic computing platforms. It is hoped that this review will shed new light on the evolution of brain-like computing.

1. Introduction

Unraveling the nature of how the brain works has long been a fascinating and challenging endeavor. The human brain is a huge neural network in which billions of neurons interconnect through trillions of synapses (**Figure 1**a–d). Benefiting from vast connectivity, functional organizational hierarchy, sophisticated learning rules, and neuronal plasticity, the human brain can simultaneously perform different complex tasks with massive parallelism, extremely low power consumption, superior fault tolerance, and strong robustness.[1] Scientists have thus been inspired to dedicate countless hours to the development of artificial intelligence (AI) as computationally powerful as the brain. A high-performance AI chip (Figure 1e) is needed to bridge the gap between artificial computing platforms and the human brain.

Mead first proposed that building neuromorphic electronic systems utilizing biological solutions could achieve more effective and energy-efficient information processing than conventional computing systems.[2] This inspirational idea has sparked a wave of interest among neuroscientists and computer scientists in brain-like computing. To build a high-performance computing platform, both efficient algorithms and powerful computational platforms are indispensable. From an algorithm perspective, artificial neural networks (ANNs) have undergone three generations of evolution. First generation ANNs are a series of neural network models with digital input and output based on McCulloch-Pitts neurons, which typically include multilayer perceptrons, Hopfield networks, and Boltzmann machines. The second generation introduces activation functions as computational units to produce analog output. Various neural networks have been proposed to handle different tasks, such as support vector machines for classification, convolution neural networks (CNNs) for image recognition, and recurrent neural networks (RNNs) for voice recognition. Currently, the second generation of neural networks is the most popular ANN for AI design. Third generation ANNs are based on spiking neurons (Figure 1g), in which information is encoded into spatial and temporal sparse spike trains.[3–5] The development of neuronal dynamics provides new insight into the simulation of biological neurons, leading to biologically plausible neuron models with rich spiking behavior. It is believed that the event-driven and sparse communicating nature of spiking neural networks (SNNs) enable low power hardware implementation.[6,7] Owing to their brain-like architecture and information processing, SNNs (Figure 1f) are promising for high-performance neuromorphic computing systems.[3]

From a hardware implementation perspective, synaptic and neuronal computations are critical for neuromorphic computing.[8,9] Traditional implementation of synaptic plasticity and neuronal dynamics based on nonbiomimetic complementary metal–oxide–semiconductor transistor (CMOS) circuits requires higher power consumption and larger chip space to

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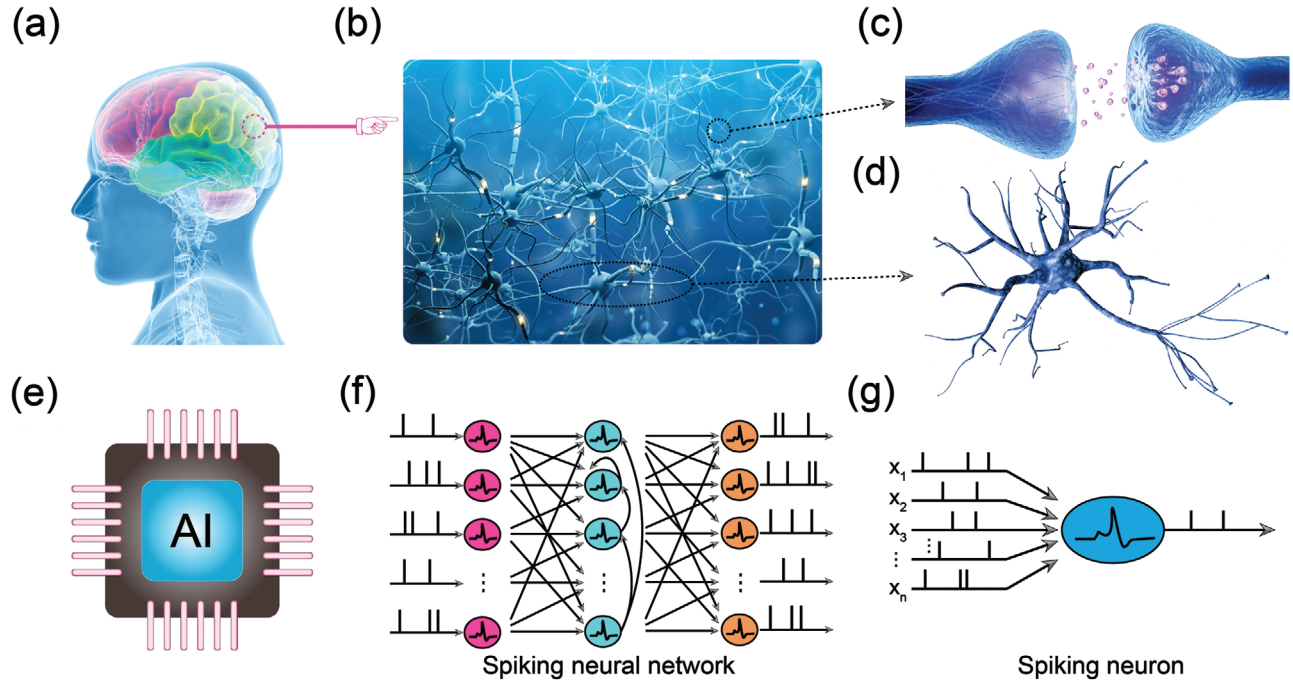

Figure 1. Schematic diagram of biological and artificial computing systems. a) The human brain. b) The biological neural network. c) A biological synapse. d) A biological neuron. e) An AI chip. f) Spiking neural networks. g) An artificial spiking neuron. a) Adapted with permission.[231] Copyright 2020, PAIXIN. b) Adapted with permission.[232] Copyright 2020, PAIXIN.

maintain biological plausibility. With the rapid development of microelectronics and materials science, novel functional devices are emerging, shedding new light on high-performance neuromorphic computing systems.[8] Various artificial synapse[10–18] and neuron[19–26] models have been developed using emerging neuromorphic devices. Mimicking the architecture and working scheme of the brain, a spike-based AI system can be implemented for brain-like computing through cooperation of vast amounts of artificial synapses and neurons.[27] Owing to the event-driven nature of spiking neurons, the overall power consumption of spike-based systems can be reduced effectively compared to general neural network computing platforms.[6,27]

In recent years, there have been many reviews that study neuromorphic computing from the perspectives of device physics,[8,28,29] circuit design,[30,31] and network integration,[27,32] promoting the development of this emerging field. Our manuscript differs from the existing literature in that the biological knowledge and a relatively systematic introduction about this field is supplied. At the same time, compared with traditional neural networks such as CNNs and RNNs,[9] this manuscript mainly focused on the introduction and implementation of SNNs, which aim to mimic the structure and information communication of the biological nervous system to realize highly efficient data processing. To provide readers a fundamental and systematic insight into brain-inspired neuromorphic computing, this review gives a comprehensive overview on the development of neuromorphic engineering from biological nervous systems to spike-based neuromorphic computing platforms. Starting with the biological nervous system (Section 2), we briefly introduce fundamental knowledge pertaining to the structures and working mechanism of biological neurons and synapses. The development and hardware implementation of artificial synapses and neurons are then reviewed in Section 3. Finally, we highlight some remarkable progress toward building SNN neuromorphic hardware systems (Section 4).

2. Biological Nervous Systems

The nervous system in vertebrates is responsible for the regulation of physiological activities, which is divided into the central nervous system (including brain and spinal cord) and peripheral nervous system (including cranial and spinal nerves). For humans, the nervous system possesses approximately 86 billion neurons, 99.9% of which are distributed in the brain.[33,34] Owing to the preeminent cognitive abilities of the brain, humans can perform many complex tasks (e.g., symbolic thought and grammatical language), which make them distinct from other primates.[33,35] The brain is a complex network composed of billions of neurons interwoven through synapses. We will provide a brief introduction to the structures and working mechanism of biological neurons and synapses in the following sections.

2.1. Brief Introduction to Neurons

To better understand the complexities involved in building ANNs, we need to first have a deep understanding of how biological neurons work. Neurons are highly specialized cells with the ability to sense stimuli and conduct nerve excitation, acting as the basic structural and functional units of biological

nervous systems. As illustrated in **Figure 2**a, a typical neuron is composed of three main structures (dendrites, soma, and axon; specific functions are described in Sections 2.1.1–2.1.3) and it can be roughly divided into two regions (somatodendritic and axonal).[36]

A neuron connects to hundreds or thousands of other neurons via synapses, and it receives and summates multiple stimuli transmitted from presynaptic neurons in the somatodendritic region and therefore generating local gradient potentials (excitatory/inhibitory postsynaptic potentials, EPSPs/IPSPs). The resulting membrane potential changes lead to on–off behavior of voltage-gated ion channels at the axon initial segment (AIS), which generates action potentials that are determined by the firing threshold. Generated action potentials are then transmitted along the axon to the nerve terminals, resulting in the activation of voltage-gated calcium (Cav) channels. Note that in the case of myelinated axons, action potentials are transmitted between the nodes of Ranvier in a way of saltatory conduction to reach nerve terminals under the assistance of voltage-gated sodium (Nav) and voltage-gated potassium Kv7 (KCNQ) channels.[37] Finally, the action potentials trigger the nerve terminals to release neurotransmitter to influence the postsynaptic neurons. By generating action potentials with consistent amplitude and different frequencies, and delivering action potentials from one neuron to another through synapses, neurons within the human brain form an intricate and vast neural network that can process a variety of complex tasks such as object recognition and language processing.

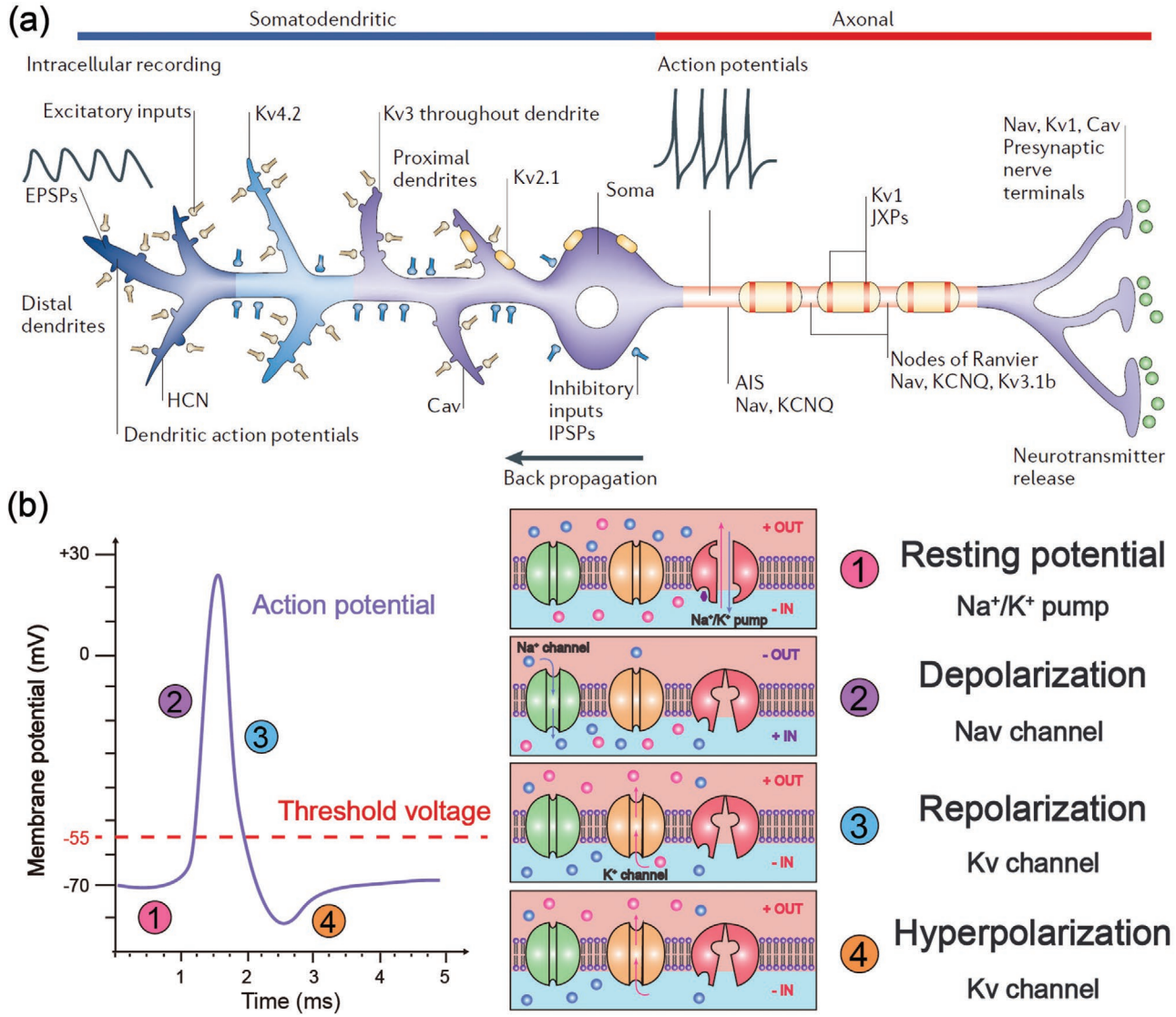

Figure 2. Schematic illustration of the fundamental structure of a biological neuron model and the corresponding molecular basic of generating an action potential. a) A neuron receives stimulations at the dendrites and generates action potentials propagating along the axon when the membrane potential overshoots a certain threshold voltage. In this process, the ion channels in different parts of the neuron interact to participate in the generation of action potentials. b) The generation of an action potential which can be divided into four stages, including resting potential, depolarization, repolarization and hyperpolarization. The Na^+/K^+ pump is responsible for restoring resting potential. The activation of Nav channel leads to depolarization. The Kv channel is responsible for repolarization and hyperpolarization. a) Adapted with permission.[36] Copyright 2006, Springer Nature.

2.1.1. Dendrites

Morphologically, dendrites are short, branching projections that protrude from the cell body of a neuron (Figure 2a). Various morphologies and synaptic properties of dendrites are essential in determining the computational functionality of neurons in the central nervous system.[38] Dendrites typically integrate synaptic inputs spatiotemporally and generate action potentials in specific patterns locally. Although the molecular mechanisms by which dendrites function have been explored extensively, the role that dendrites play in neural network computations requires further investigation.[39] Studies have revealed that dendrites exhibit a mass of nonlinear responses such as Nav, Cav, NMDA spikes, and calcium-induced calcium release.[40–43] Recently, Beaulieu-Laroche et al. performed calcium imaging of dendritic and somatic compartments of L5 neurons in the primary visual cortex under awake conditions, revealing that the degree of participation of dendrites in the neural information processing is unexpected. Experimental results indicate strong coupling between dendritic and somatic activity. Dendrites act like antennas, assisting neurons to monitor instructions from neighboring neurons.[44] More recently, according to studies on dendritic function in recent years, Payeur et al. delineated four classes of dendritic information processing as spatiotemporal filtering, information selection, information routing, and information multiplexing.[45] The knowledge gained from these studies has influenced creative design strategies toward the development and optimization of dendritic computational neural networks.

2.1.2. Soma

Soma (also referred to as the cell body of a neuron) is the vegetative center of a neuron that contains the cell nucleus and organelles. Depending on the type of neuron, soma can be found in a variety of shapes (e.g., star, conical, spherical, and pear-shaped). The soma is responsible for synthesizing neurotransmitters and integrating electrical signals received by dendrites to determine whether an action potential is generated or not.

2.1.3. Axon

The axon is connected to the soma, acting as the output channel of neural signals in biological neurons. Resulting from the activation of Nav channels, action potentials are initialized at the AIS and then propagate along the axon to the nerve terminals. An axon may extend for a considerable distance with a constant diameter, and it does not form synaptic structure before termination. It has to ensure the long-distance transmission of neural action potentials for normal communication between neuron cells. Scientists have made great strides studying the complicated process of axonal transport to better understand the structure and function of axons.[46,47] Since Weiss and Hiscoe first revealed the movement of matters in axons, two main experimental approaches have been developed to facilitate the study of axonal transport: the use of radioactive precursors to pulse-label axon-transported materials and imaging techniques for the direct observation of transport in living axons.[47–49] The development of new techniques provides higher resolution to observe the movement of axonal materials, thus deepening our understanding of axonal transport.

Figure 2b describes the change of the membrane potential when an action potential is generated, and the related molecular basis of the electrical activity. An action potential can normally be roughly divided into four segments: resting potential, depolarization, repolarization, and hyperpolarization.[50] When the neuron is silent, the membrane potential is in a relatively steady state (resting potential) under the effect of Na^+/K^+ pump, termed polarization. When the membrane potential undergoes potentiation, the Nav channel is activated under the potential gradient, resulting in a rapid influx of Na^+. When this occurs, the polarity of the membrane potential changes from negative to positive, leading to depolarization of the membrane potential. The physiological processes of repolarization and hyperpolarization are dominated by voltage-gated potassium (Kv) channels, which allow K^+ to flow out of the cytomembrane to restore the normal membrane potential of neuron cells. Finally, the ion concentration inside and outside the cytomembrane is restored to an equilibrium state regulated by the adenosine triphosphate (ATP)-driven Na^+/K^+ pump. Note that when a single suprathreshold stimulus causes the cell to generate an action potential, the cell membrane will not normally respond to subsequent stimuli until the membrane potential returns to the resting potential, referred to as the refractory period.[51,52]

2.2. Brief Introduction to Synapses

Neurons are the basic units of information processing in the brain and in order to form a synergistic and efficient neural network, they need to communicate with each other. The synapse concept was first proposed by Sherrington in 1897 to describe the functional connection between neurons in the central nervous system. Since then, extensive investigations have been performed to elucidate how synapses work, gradually unraveling the mysteries of the nervous system.

2.2.1. Synaptic Transmission

A synapse typically consists of a presynaptic membrane, synaptic cleft, and postsynaptic membrane. It is generally recognized that there are two main types of synaptic transmission: chemical and electrical.[53–55] **Figure 3**a,b schematically illustrates these two types of synapses.

In chemical synapses (Figure 3a), information is converted from electrical signals to chemical signals by releasing neurotransmitters from the presynaptic membrane into the synaptic cleft. Intricate presynaptic molecular machinery is required to regulate the release of neurotransmitters when action potentials arrive. Neurotransmitters then react with receptors in the postsynaptic membrane of adjacent neurons to convert chemical signals into electrical signals; sophisticated postsynaptic molecular machinery is responsible for detecting and translating the received chemical signals into postsynaptic potential signals.

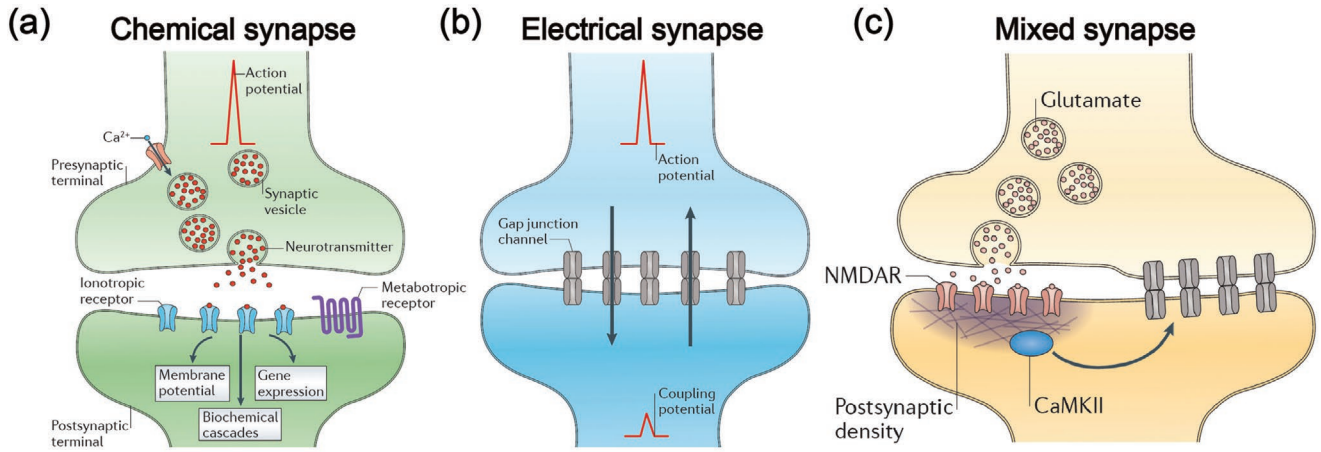

Figure 3. Main modalities of synaptic transmissions. a) chemical synapse. The arrival of action potential results in the activation of voltage-gated Ca^+ channels, promoting the probabilistic release of neurotransmitters by exocytosis from presynaptic membrane. The ionotropic and metabotropic receptors on the postsynaptic membrane can detect and translate the information carried by neurotransmitters into different postsynaptic behaviors, varying from changes in membrane potential to gene expression. b) Electrical synapse. Electrical transmission is conducted by gap junctions (some clusters of intercellular channels) between two adjacent cells. The transmission is bidirectional: when an action potential is transmitted from pre-synapse to postsynapse, the postsynaptic resting potential propagates concurrently to the pre-synapse. c) Mixed synapse. Chemical and electrical transmission coexist at mixed synapses. Chemical synapses (such as glutamate-based) influence the connective strength of electrical synapses by activating the NMDA receptors and CaMKII. a–c) Adapted with permission.[55] Copyright 2014, Springer Nature.

Therefore, with neurotransmitters as the medium, information can be transmitted between neurons in a fraction of a millisecond.[55] These superior characteristics make chemical synapses robust and adaptable to different functional requirements. Since neurotransmitters can only be released from the presynaptic membrane, signal transmission in chemical synapses is unidirectional (presynaptic neurons to postsynaptic neurons, but not vice versa).

The direct connection of adjacent neuronal interiors with gap junctions (clusters of intercellular channels) permits the bidirectional transport of electrical currents, ions, and small molecules in electrical synapses (Figure 3b).[56] Although electrical synapses allow small metabolites to pass through, they fail to amplify and transform the afferent presynaptic signal, thus differing from chemical synapses. Electrical transmission exhibits higher reliability and faster transmission speed, which are both crucial in the escape response networks of animals.[57,58] A recent study identified neuronal gap junctions of electrical synapses between auditory afferents and Mauthner cells of goldfish that are molecularly asymmetric, which is similar to chemical synapses.[59] This molecular asymmetry accounts for the rectification effect of electrical transmission, promoting the cooperativity between different neurons.[59–61]

Although interactions between chemical and electrical synapses in the nervous system have aroused considerable attention, relevant studies elucidating their interplay remain scarce. Interestingly, mixed synapses (Figure 3c) were discovered at the terminations of primary auditory afferents on the teleost Mauthner cells, advancing our understanding of the interactions between these two modalities of synapses.[55,62–64] Utilizing confocal microscopy and freeze-fracture replica immunogold labeling, Pereda et al. found connexin35 (Cx35) in abundance and the NR1 subunit of the NMDA glutamate receptor at these mixed synapses, revealing the underlying interaction between chemical and electrical transmissions.[63] When a presynaptic membrane releases glutamate, NMDA receptors in the postsynaptic membrane receive neurotransmitters that lead to potentiation of the postsynaptic potential, resulting in an increase of calcium levels and activation of calcium/calmodulin-dependent protein kinase II (CaMKII) (CaMKII is abundant at chemical synapses).[65,66] Next, CaMKII regulates electrical transmission, leading to the potentiation of electrical synaptic conductance.[65] Interactions between electrical and chemical synapses have also been discovered to be relative to brain insult in adult mammals.[67,68]

2.2.2. Synaptic Plasticity

Synapses are not solely conveyers of information between neurons, but also participants in the information processing of biological nervous system.[69] Many experimental studies show that synapses exhibit activity-dependent characteristics during neural activities, which is enlightening for understanding the working mechanism of brain computation.[70–76] The phenomenon of synaptic plasticity is the foundation of learning and memory of biosystems, which refers to how the connective strength, functionality, and efficiency of a synapse are influenced for a short or long time by the temporal relationships between presynaptic and postsynaptic activities.[77–79] Generally, synaptic plasticity can be roughly divided into two categories: i) long-term plasticity, which involves the changes on synapses that last for hours or longer, is usually thought to be critical for learning and memory in mammals;[70,71,78,80] and ii) short-term plasticity, which represents some activity-dependent characteristics on the tens of milliseconds to several minutes time scale.[74,81] Each type of synaptic plasticity can be further subdivided into many subclasses that exhibit different electrophysiological phenomena to some extent.

Long-term plasticity we mentioned usually includes long-term potentiation (LTP) and long-term depression (LTD). LTP is a persistent enhancement phenomenon in the signal transmission of two neurons that occurs when the synapses are excited by excessively strong stimulation.[71] In 1973, Bliss and Lømo first observed LTP phenomenon in the dentate area of the hippocampus of rabbit, whereby the amplitude of postsynaptic potentials increased after repeated high-frequency electrical stimulation.[70] Subsequently, LTD, the opposite of the LTP effect, was found in the hippocampus by Lynch et al., who observed a depression of the target cell to a second stimulation after the potentiation of one afferent.[80] Because both LTP and LTD were found in the hippocampus, a region associated with memory storage, neuroscientists were excited and put forth significant effort to reveal the relationship between synaptic plasticity and memory.[78,82,83] Spiking-timing-dependent plasticity (STDP) is a typical form of long-term plasticity, which brings about LTP and LTD according to the relative temporal relationship between presynaptic and postsynaptic activities.[84] It is one of the most important working principles to address time-dependent computing tasks of the nervous system. The working principles of STDP will be discussed in detail in Section 4. Long-term plasticity plays an indispensable role in biological neural activity. For instance, drugs addiction, a major clinical problem caused by drugs abuse, is a manifestation of long-lasting memory.[85,86] Studying how drugs affect synaptic plasticity in specific areas of the brain is therefore beneficial for addressing some intractable health problems of society.

Short-term plasticity is essential for the nervous system to perform complex computation tasks, involving a series of neural activities that mediate the connective strength of synapses on the tens of milliseconds to a few minutes time scale.[74,81] Likewise, depending on the alteration of synaptic strength, it can also be grouped into two categories: short-term potentiation (STP) and short-term depression (STD). Paired-pulse facilitation (PPF) is a typical phenomenon of short-term synaptic enhancement on the hundreds of milliseconds time scale, which is common in many chemical synapses.[87] It manifests more remarkable EPSPs when the second of two consecutive stimuli (usually 20–200 ms) is evoked. It is generally believed that residual free Ca^{2+} in the intra terminal of the presynaptic neuron caused by the first stimulation promotes the release of neurotransmitter excited by the second spike, resulting in increased neuronal excitability.[74] Conversely, if the postsynaptic potentials (PSPs) evoked by the second stimulus is lower than the previous one, the effect is known as paired-pulse depression (PPD). As the frequency and number of action potentials increases, the enhancement of synaptic strength can last for tens of seconds or even minutes, which is referred to as post-tetanic potentiation.[88]

In addition to the aforementioned synaptic plasticity, there are also many other kinds of plasticity that are essential for synaptic computation and neural signals processing, such as spiking-rate-dependent plasticity (SRDP), nonassociative learning, associative learning, synaptic scaling, and synaptic redistribution.[89–91] It is worth emphasizing here that revealing the nature of synaptic plasticity is crucial to understanding the working mechanisms of biological nervous systems, which in turn promotes the development of neuroscience.

3. Artificial Synapses and Neurons

The human brain is a neural network with neurons as computing units and synapses as connected nodes. Through the collaboration of synapses with different forms of synaptic plasticity and neurons with diverse functions, the brain can easily and efficiently complete complex tasks such as object recognition and speech identification which are too difficult and power-hungry to be executed by traditional computer systems. Motivated by the efficient information processing of biological nervous systems, scientists are devoted to the development of brain-inspired machines to tackle the well-known von Neumann bottleneck.[92] Building robust and functional artificial synapses and neurons is critical for the construction of SNNs. In the following sections (Sections 3.1 and 3.2), we review the development of hardware implementation of artificial synapses and neurons, which lays a solid foundation for understanding the working principles of spike-based neural networks discussed in Section 4.

3.1. Artificial Synapses

Synapses are one of the most pivotal building blocks in neural networks and it is of great importance to develop artificial synapses both theoretically and practically. When it comes to developing SNNs on hardware, the simulation of biomimetic synapses and synaptic plasticity is the first step necessary to achieve this goal. In recent years, neuromorphic devices have emerged with the development of nonvolatile technologies (**Figure 4**). They are ideal devices for synapse simulation, owing to their incredible ability to mimic complex synaptic plasticity and synaptic efficacy in a single device. In biology, the connective strength of a synapse (referred to as the synaptic weight in electrical circuits) determines the correlative relationship between two neurons, which can be subtly represented by the conductance of neuromorphic electronics. Versatile devices such as two-terminal memristors and three-terminal floating-gate transistors have been proposed to mimic diverse synaptic functions, including STP/LTP, PPF/PPD, SRDP, and STDP.[10–18,93–99] Owing to its nonvolatile nature, the synaptic weight of a nonvolatile neuromorphic device can theoretically be regulated and maintain for a certain period of time that depends on the history of the applied external stimuli. This feature is quite analogous to the activity-dependent regulation of synaptic plasticity in biology. With collaborative efforts between researchers in the electronics and neuroscience communities, synaptic plasticity has been realized in emerging devices. Based on these advancements, more compact, efficient, and lower energy-consuming synaptic circuits are expected to be developed in the near future.

Proposed by Leon Chua in 1971, the two-terminal memristor is the fourth fundamental circuit element, and it is one of the most promising candidates for neuromorphic computing.[100,101] It has been discussed intensively because it exhibits many advantageous properties (e.g., nanosecond level response times, repeatable and stable conductance regulation, outstanding scalability, low energy consumption, CMOS technique compatibility, and space efficient configuration) that make it desirable

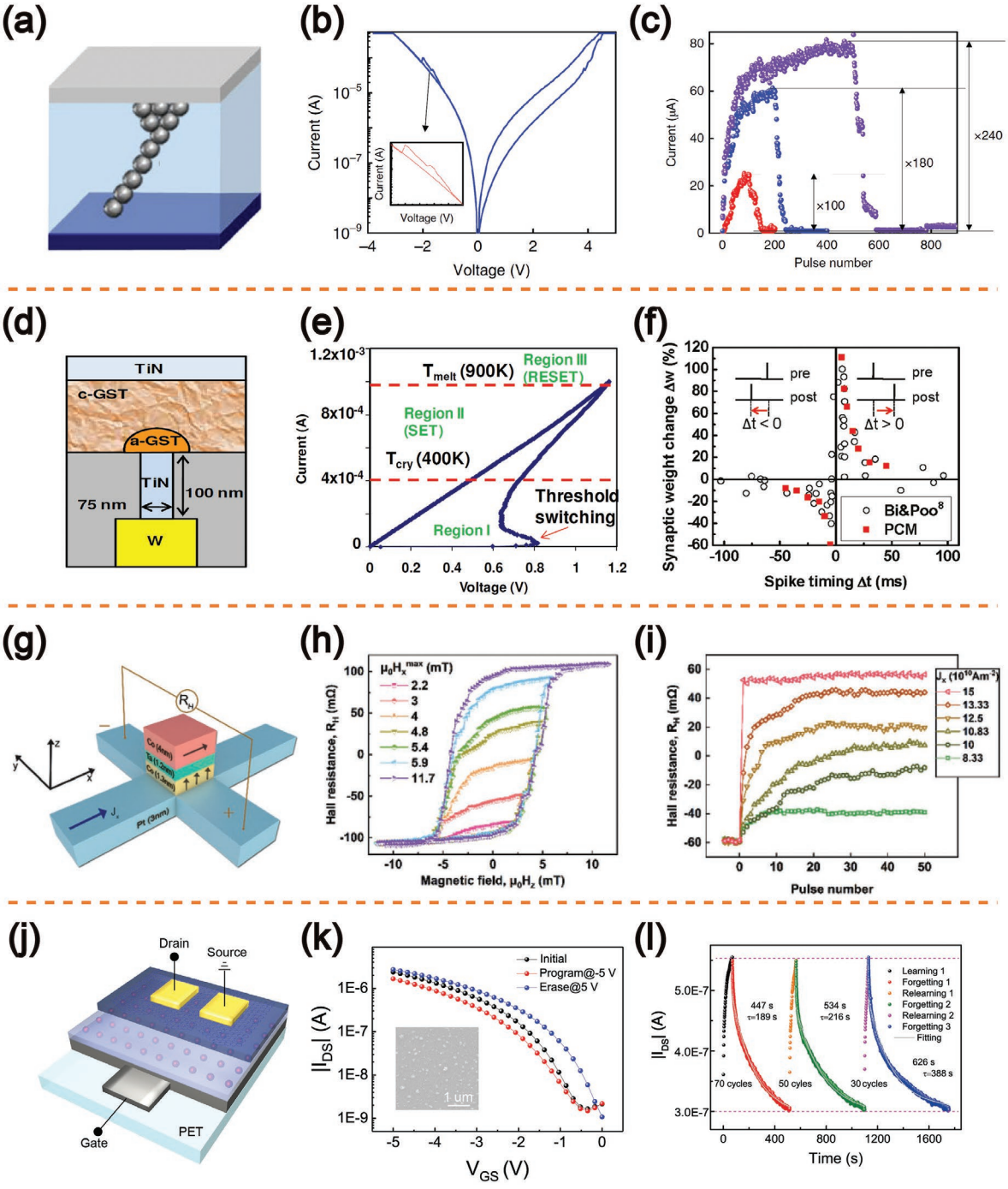

Figure 4. Artificial synapses based on neuromorphic devices. a) A conceptual diagram of a two-terminal memristor. b) Typical current–voltage (*I–V*) properties of the memristor. c) Conductance potentiation and depression of the synaptic device. A pulse train comprises sequential 100/200/500 set pulses (5 V, 5 μ s) followed by sequential 100/200/500 reset pulses (–3 V, 5 μ s) was applied to the device, and the response current was read at (2 V, 1 ms) pulse after each set/reset pulse. The analog on/off ratios are × 100, × 180 and × 240 at 100-100, 200-200, and 500-500 potentiation-depression pulses, respectively. a–c) Adapted with permission.[14] Copyright 2018, Springer Nature. d) Schematic diagram of a phase change cell. e) *I–V* characteristics of a PCM cell. f) Implementation of STDP with PCM cells. The change of synaptic weights is described as a function of the relative time difference between presynaptic and postsynaptic spikes. Experimental data is shown together with the one measured by Bi and Poo in biological hippocampal glutamatergic synapses. d–f) Adapted with permission.[15] Copyright 2012, American Chemical Society. g) Device structure of a double magnetic layered system and the definition of *x–y–z* coordinates for experimental measurement. h) R_H–H_z loops with $\mu_0 H_z$ sweeping from –11.7 mT to $\mu_0 H_z^{max}$ and then back to –11.7 mT. i) R_H varies with the number of current pulses (total 50) in different constant magnitudes J_x. The R_H is measured 2 s after each pulse. g–i) Adapted with permission.[123] Copyright 2019, Wiley-VCH. j) Schematic of a bottom-gate top-contact flexible synaptic transistor. k) Typical transfer plot of the flexible synaptic transistor with 0.15 wt% C_{60}. Inset: Corresponding top-view SEM image of the C_{60}/PMMA hybrid film utilized in the synaptic transistor. l) Implementation of physiological learning, forgetting, and relearning processes with the proposed C_{60}-based device. j–l) Adapted with permission.[17] Copyright 2018, Wiley-VCH.

for practical applications.[28,102–104] Interestingly, owing to their intrinsic ion migration dynamics, memristors are capable of emulating important synaptic plasticity behaviors that are essential for building SNNs. Aono and co-workers successfully emulated the synaptic plasticity of both STP and LTP with a Ag_2S inorganic memristor that exhibited dynamic memorization similar to biological synapses and other interesting behaviors such as the physiological process of memorizing and forgetting in biology, demonstrating a breakthrough in the simulation of synapses.[105] A Ag/AgInSbTe/Ag memristor with reproducible continuous conductance modulation was utilized to mimic bidirectional Hebbian plasticity, which is one of the fundamental principles of neural computation in biological systems.[12] At the same time, synaptic saturation was also observed in this chalcogenide memristor-based electronic synapses, which is a significant adjustment of Hebbian rules to stabilize the growth of synaptic weight. By utilizing the formation and rupture mechanism of Ag conductive filaments, Lu et al. developed a synaptic memristor with repeatable conductance potentiation and depression. STDP characteristics similar to their biological counterparts were successfully obtained, offering a potential option for efficient synaptic computing.[106] Hardware implementation of STDP has long been a challenge because of the influence of the initial conductance on the adjustment of synaptic weight. Interestingly, self-adaptive STDP behavior was first demonstrated by Strukov et al. using metal-oxide memristors.[107] Stable and insensitive initial state synaptic plasticity was exhibited by these metal-oxide memristors, which is beneficial for building reliable large-scale neuromorphic networks. Synaptic competition and cooperation have been considered to be significant to the regulation and stabilization of biological neural networks.[108,109] Inspired by the highly anisotropic ionic transport properties of 2D MoS_2, an ionic-electronic coupled memristor system was proposed to emulate synaptic competition and cooperation in biology.[13] With Li^+ ion migrating in the in-plane direction under the control of an electric field, MoS_2 undergoes reversible, local phase transitions between the semiconducting 2H phase (trigonal prismatic structure) and metallic 1T' phase (octahedral structure), leading to reliable memristive behavior of the Au/Li_xMoS_2/Au synaptic device. Synaptic competition and synaptic cooperation behaviors have been successfully emulated through the reasonable design of device connections and operation schemes. Recently, Kim et al. designed an artificial synaptic chip containing a single-crystalline SiGe layer that can precisely control the synaptic weights of analog resistive switching devices (Figure 4a–c), comparable to how neurons quantify the amount of neurotransmitter released into the synaptic cleft.[14] Utilizing threading dislocations in SiGe, the conductive filaments in the active layers were confined to a 1D channel, resulting in a distinct enhancement of homogeneity and stability of synaptic devices, taking a further step toward artificial synapse simulation.

Since the discovery of resistive switching phenomenon upon the phase change of chalcogenide materials, phase-change materials (PCMs) have been extensively developed in the field of nonvolatile techniques owing to their superior characteristics, such as high reliability, multiple and repeatable conductance states, and low device-to-device variation.[110–112] PCMs usually have two different lattice structures in resistive switching devices: a crystalline phase (long-range order) and an amorphous phase (long-range disorder), corresponding to the low resistance state (LRS) and high resistance state (HRS), respectively.[112] The resistance states of phase-change memory can be subtly mediated by applying consecutive voltage pulses, which result in the change of temperature and therefore the lattice structure transition of PCMs. As one of the most mature emerging nonvolatile memory technologies, phase-change memory has been increasingly utilized for electronic synapses in neuromorphic systems in recent years. A single PCM-based electronic synapse was firstly reported to implement both modulation of the time constant of STDP and the realization of various STDP kernels with energy consumption at the picojoule level (Figure 4d–f).[15] It is found that nucleation-dominated GeSbTe exhibits more gradual regulation of conductance, whereas growth-dominated GeTe tends to behave an abrupt conductance change, indicating the LTP behavior of PCM-based synapses can be controlled by tailoring the crystallization state of PCMs.[113] In order to deal with the asymmetry of LTP and LTD behaviors in PCM-based synapses, a 2-PCM synapse circuit architecture was proposed, in which the read, write, and reset operating schemes are well optimized, making the synapse a versatile component for large-scale neural network simulations. This synapse model was also demonstrated on a two-layer SNN for simulating complex visual pattern extraction with a satisfactory accuracy of 92%. In the same year, Wong et al. proposed two different spike schemes (based on impulse sequence and single pulse) and implemented symmetric and asymmetric STDP in PCM synapses to investigate their characters in RNNs.[16] Taking the advantage of the asymmetric plasticity when converting temporal information into spatial information, and symmetric plasticity in storage and recall of specific patterns, the authors performed sequence learning and associative learning respectively, which is a meaningful exploration of the brain-like learning. Later, they further implemented associative learning and pattern recognition at the hardware level with a 10×10 PCM-based synapse array, taking a significant step toward the construction of brain-like neural networks. The pioneering work of Bhaskaran et al. introduced a fully integrated all-photonic synapse system that combines PCMs with silicon nitride waveguides to realize the well-known Hebbian Learning Rule that is crucial for neuromorphic computing.[114] The structure design and use of finite element method (FEM) simulations resulted in optical synapses that exhibited many excellent properties, such as ultrafast operation speed, no electrical connection energy losses, and virtually infinite bandwidth. These exciting results provide new insights for the design of artificial hardware nervous systems.

Spin-transfer torque magnetic random-access memory (STT-MRAM), a novel non-volatile technique operated through magnetization reversal in the magnetic tunnel junctions (MTJs), is a second generation of MRAM.[115,116] A typical MTJ contains a magnetic pinned layer (PL), a magnetic-free layer (FL), and an insulator layer sandwiched between the other two magnetic layers. The magnetization orientation of the PL is pinned, whereas the magnetic FL can be switched according to the current direction. The parallel and antiparallel alignment of magnetization between two magnetic layers leads to the LRS and HRS of the MTJ. Kano et al. first reported a 4k bit Spin-RAM

circuit with a STT-MRAM cell based on a 1-transistor and a 1-MTJ (1T1J) structure.[117] In contrast to a current-induced magnetic field, directly injecting spin polarized electrons is more efficient to reverse the orientation of the magnetic layer, bringing about the superior electrical performance such as low power and high operation speed. However, the switching stochastic effect of the STT-MRAM is considered to be a drawback for reliable programming.[118] Querlioz et al. developed a theoretical model to analyze the switching time of the MTJ, and the model fitted well with the experimental data.[119] They further performed system-level simulations of a spiking neural network with STT-MTJs as stochastic memristive synapses, and the Monte Carlo simulations showed the robustness of the proposed learning system to device variations.[120,121] Recent work of Appenzeller et al. introduced a new spin–orbit torque (SOT)-MRAM-based compound synapse consisting of stochastic binary components for neuromorphic computing. By adopting appropriate pulse scheme, linear potentiation and depression of the synaptic weights were successfully demonstrated, which effectively improved the recognition rates of the MNIST patterns during deep belief network (DBN) simulations.[122] Tuning the efficacy of the SOT by the in-plane field component can broaden a binary ferromagnet device into an analog synapse with multistate (Figure 4g–i).[123] A current pulse was utilized to manipulate the orientation of the magnetic material to successfully demonstrate EPSP, IPSP, and STDP. The study provides new insights into spintronic synaptic emulation for neuromorphic computing systems.

As one of the most mature techniques in modern microelectronics, three-terminal transistor-based devices are extensively applied to build artificial synapses because they possess a number of advantages, including reliability, homogeneity, and CMOS technique compatibility.[124–127] At the same time, the gate-tunable channel conductance of transistor-based devices bears a remarkable resemblance to biological synapses, whereby the connective strength (synaptic weight) is regulated by neurotransmitters released from the presynaptic membrane by exocytosis effect, making it a feasible option for synaptic simulation. Han et al. reported a solution-processed C_{60}-based synaptic transistor that concurrently exhibited signal transmission and learning functions (Figure 4j,k).[17] Benefiting from the ambipolar trapping properties of C_{60} and reasonable device optimization, the fabricated synaptic transistor demonstrated considerable electrical performance with a 2.95 V memory window, a 10^3 current on/off ratio, and over 500 times endurance cycle. Comprehensive biological synaptic plasticity (e.g., EPSC, STP/LTP, PPF/PPD) and repeatable learning–forgetting process (Figure 4l) were also successfully emulated using the as-fabricated synaptic transistors. This work has furnished an avenue to prepare flexible, solution-processable, low operation voltage transistor-based artificial synapses.

An ion-gated synaptic transistor with a three-terminal planar configuration was reported to exhibit tunable synaptic dynamics.[99] $LiClO_4$ dissolved in polyethylene (PE) was dropped above the semiconducting channel and side gate regions to provide Li^+ migration under the control of the side gate, which is in direct contact with the polymer electrolyte. Li^+ adsorption and intercalation in the 2D van der Waals semiconducting channel resulted in tunable synaptic dynamics, such that STP occurs when stimulation is insufficient, while LTP happens under excessive stimulation. The authors ascribed the transition from STP to LTP to the spontaneous backward diffusion of Li^+ adsorbed on the 2D semiconducting channel and intercalation of Li^+ into the channel. A systematic investigation using density functional theory (DFT) and transmission electron microscopy (TEM) revealed that WSe_2 switched between a metallic phase and a semiconducting phase, depending on whether or not Li^+ intercalates in the 2D materials. A high-performance electrochemical synaptic device was reported to exhibit low power operation (<10 pJ for a 10^3 μm^2 device) and linear and nonvolatile conductance regulation (>500 distinct states).[128] Furthermore, the authors also provided a feasible scheme for low-cost fabrication of an all solid-state plastic device with commodity polymers, indicating the potential for use in stretchable and implantable electronic systems. Compared with traditional unipolar transistor, ambipolar transistors allow simultaneous transport of positive and negative charge carriers in a single semiconducting channel, which can effectively extend the dynamic modulation range of synaptic weights.[129] Ambipolar transistors have been used to construct reconfigurable artificial synapses with excitatory and inhibitory modes in a single device, thus expanding the functionality of artificial synapses for intelligence systems.[130,131] Furthermore, photonic synapses based on transistor-based devices have provided new insight into improving the working efficacy of synapse networks, paving the way for intelligent optoelectronic computing systems.[127,132,133]

Table 1 summarizes representative works on artificial synapses with different emerging devices in terms of device structure, device size, retention, endurance, reproducibility, synaptic plasticity implemented, CMOS compatibility, etc. Different schemes for synaptic function simulation possess their own insufficiencies, which need to be taken into account and optimized in future designs. Due to the nature of the conductive filament mechanism, the main obstacle to the development of ionic memristors is the reliability and uniformity of devices, requiring the development of more advanced device fabrication technologies to address these problems. For instance, by introducing epitaxial threading dislocations to confine the formation of conductive filaments, the switching uniformity can be well controlled.[14] For phase-change devices, time-dependent resistance drift phenomenon is a problem that needs to be solved.[134] It is of great significance to reduce the drift coefficient by optimizing the fabrication of PCMs. MRAM-based devices are mainly limited by a small memory window, which results in a relatively small and nonlinear dynamic range of synaptic weight. Hence, it requires complicated peripheral circuit to read the signals, leading to noise sensitivity. Appropriate design of device connection[135] and suppression of defect-induced localized states[136] are optional methods to improve the on/off ratio. Although synaptic transistors can provide more stable operation, many devices based on novel materials (e.g., 2D materials, organic polymers, and perovskite materials) and novel operating principles (e.g., electrochemical doping, ion intercalation, and electrical double layer gating) suffer from poor scalability, ultimately limiting their large-scale applications. These shortcomings will need to be addressed in the future to advance synaptic transistor development.

Table 1. A brief summary of some representative artificial synapses based on neuromorphic devices.

Type	Structure	Dimensions (D or $W \times L$)	Retention/endurance	Reproducibility	Synaptic plasticity	CMOS compatibility	Refs.
Ionic memristor	$Pt/Ag_2S/Ag$	–	$>2 \times 10^4$ s/-	49	STP, LTP	–	[105]
	Ag/AgInSbTe/Ag	$100 \times 100\ \mu m^2$	>2200 s/-	21	SRDP, STDP	–	[12]
	$Au/Li_xMoS_2/Au$	–	>7000 s/$>10^3$	–	Synaptic competition and cooperation	No	[13]
	Ti/Au/Ag/Pd/i-SiGe/p-Si	$5 \times 5\ \mu m^2$	>48 h/$>10^6$	100	–	–	[14]
	Au/SiO_xN_y:Ag/Au	$10 \times 10\ \mu m^2$	-/$>10^6$	–	STP, LTP, SRDP, STDP	–	[137]
	$Pt/TiO_2/Pt$	–	>2.5 h/>500	–	LTD, LTP, STDP	–	[138]
	$W/HfO_y/HfO_x/Pt$	$D = 50\ \mu m$	$>10^4$ s/10^3	10	LTD, LTP, SRDP, STDP	–	[139]
Phase-change memory	$TiN/Ge_2Sb_2Te_5/TiN/W$	$D = 75$ nm	-/$>10^7$	–	STDP	Yes	[15]
	$W/Ge_1Cu_2Te_3/W$	$D = 500$ nm	-/3×10^3	–	STDP	Yes	[140]
MRAM-based	Ta/CoFeB/MgO/Ta	$2.36\ \mu m^2$	–/–	–	–	Yes	[122]
	Pt/FM1/Ta/FM2	$6 \times 6\ \mu m^2$	$>1.8 \times 10^4$ s/-	–	EPSP/IPSP, STDP	–	[123]
Transistor-based	C_{60} floating gate	$1000 \times 50\ \mu m^2$	>1000 s/>500	–	PPF, PPD, STP, LTP	–	[17]
	Ion gated 2D vdW based	$L = 1\ \mu m$	>5000 s/-	–	STP, LTP	No	[99]
	Electrochemical organic transistor	$2.25\ mm \times 65\ \mu m$	>25 h/1.5×10^4	–	PPF, STP, LTP, STDP	–	[128]

3.2. Artificial Neurons

As the cornerstone of an AI system, artificial neurons play an indispensable role in information communication and processing, attracting widespread attention from neuroscientists worldwide for decades. In this section, we first provide a brief introduction to some well-known artificial spiking neuron models (Section 3.2.1) and then discuss in detail the hardware implementation of spiking neurons for CMOS-based circuits (Section 3.2.2) and emerging neuromorphic devices (Section 3.2.3).

3.2.1. Biological Neuron Models

Figure 5 schematically illustrates 20 of the most common spiking behaviors in biological neurons (i.e., tonic spiking, phasic spiking, tonic bursting, phasic bursting, mixed mode, spike frequency adaptation, class 1 excitable, class 2 excitable, spike latency, subthreshold oscillations, resonator, integrator, rebound spike, rebound burst, threshold variability, bistability, depolarizing after-potential, accommodation, inhibition-induced spiking, and inhibition-induced bursting).[24,141] Such diverse spiking behavior is observed in different types of neurons, indicating the abundant spiking dynamics of biological neurons for complex information exchange in the brain. Detailed descriptions of each spiking feature can be found in the references cited herein.[24,141] Neurons in different areas of the brain manifest disparate functions, and even the same neurons can make different responses according to variations in the physiological environment and external stimuli. Therefore, to build versatile, adaptive, robust, and general-purpose AI systems, it is of significant importance to develop multiple types of neuron models.

With the rapid development of neuroscience, different neuron models have been proposed to meet various requirements for neuromorphic computing. Bionic neurons can be compartmentalized into two broad categories: i) biologically plausible neurons that use explicit models to exhibit similarly complex behavior of biological neurons and ii) biologically inspired neurons, which are abbreviated models that aim to replicate critical features of biological neurons with relatively low implementation complexity.

The Hodgkin–Huxley (H–H) model, proposed by Hodgkin and Huxley in 1952, is the most well-known biologically plausible neuron model for mimicking the electrical characteristics of excitable neurons.[142] It is a mathematical model consisting of nonlinear differential equations with four state variables, which describe the change of membrane potentials with respect to time. It regards the cell membrane components as an equivalent circuit, with the lipid bilayer, voltage-gated ion channels, leak channels, electrochemical gradients, and ion pumps represented with capacitance (C_m), ionic electrical conductances (g_{Na}, g_K), linear conductance (g_L), voltage sources (E_n) and current source (I_p), respectively. Benefiting from multiple parameters and complex variable relationships, the H–H model can successfully reproduce many complicated spiking behaviors (**Figure 6**), making it valuable in the field of neuroscience. Morris and Lecar later proposed a simpler model using two nonlinear differential equations to describe the Na^+ (or Ca^{2+}) and K^+ currents that account for various oscillatory behaviors in the barnacle muscle fibers.[143] Although the Morris-Lecar model is a simplified version of the H–H model, it provides sufficient biological plausibility and complexity to adequately reproduce spiking behavior (Figure 6) to meet different computing requirements in neuromorphic systems.[144,145]

Although the H–H model can reproduce the firing behavior of biological neurons to a high degree of accuracy, it is too complex for practical applications using hardware computing systems because of the large number of parameters that need to be optimized. Therefore, a variety of biologically-inspired

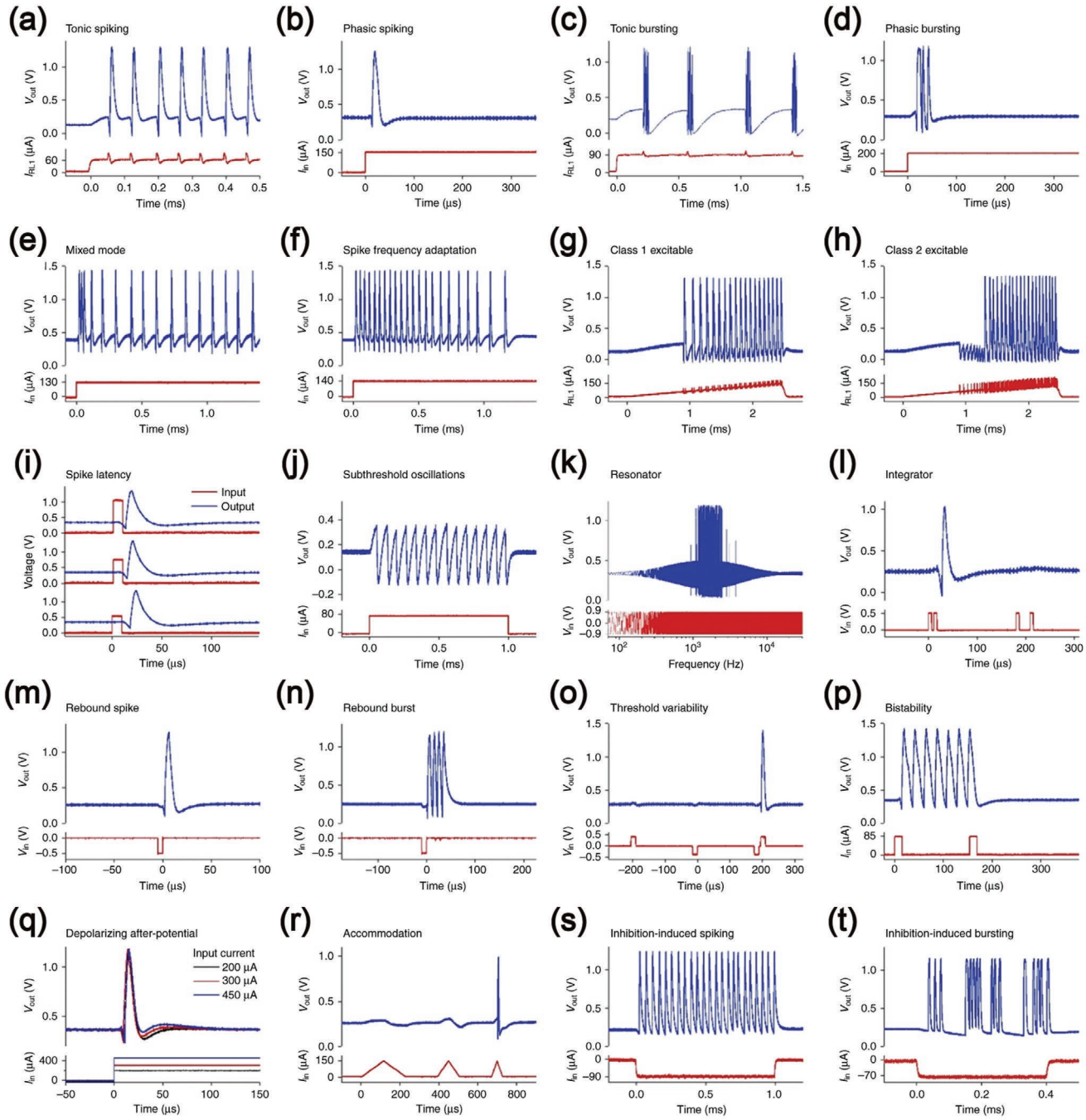

Figure 5. Schematic illustration of the 20 common biological spiking behaviors experimentally demonstrated in memristor based neurons. a) Tonic spiking. b) Phasic spiking. c) Tonic bursting. d) Phasic bursting. e) Mixed mode. f) Spike frequency adaptation. g) Class 1 excitable. h) Class 2 excitable. i) Spike latency. j) Subthreshold oscillations. k) Resonator. l) Integrator. m) Rebound spike. n) Rebound burst. o) Threshold variability. p) Bistability. q) Depolarizing after-potential. r) Accommodation. s) Inhibition-induced spiking. t) Inhibition-induced bursting. a–s) Adapted under the terms of the CC-BY Creative Commons Attribution 4.0 International license (https://creativecommons.org/licenses/by/4.0).[24] Copyright 2018, The Authors, published by Springer Nature.

neuron models have been proposed (e.g., the Fitzhugh-Nagumo model,[146,147] Hindmarsh-Rose,[148] Wilson,[149] Izhikevich,[150] and Mihalas-Niebur models[151]). The Fitzhugh-Nagumo model is a simplified version of the H–H model, consisting of two nonlinear ordinary differential equations, which are used to characterize the fast evolution of the membrane potential and the slow "recovery" effect of Na^+ channel deinactivation and K^+ channel deactivation. The Hindmarsh-Rose model is a 3D nonlinear system for bursting and thalamic neurons. Through appropriate parameter selection and optimization, most of the spiking behavior can be exhibited (Figure 5). Another less realistic but also powerful model is the Wilson model which contains four differential equations that describe the dynamics of neocortical neurons. Because it reproduces a good

Neuron models	All-or-nothing firing	Refractory period	Excitation block	Biologically-plausible	Tonic spiking	Phasic spiking	Tonic bursting	Phasic bursting	Mixed mode	Spike frequency adaptation	Class 1 excitable	Class 2 excitable	Spike latency	Subthreshold oscillation	Resonator	Integrator	Rebound spike	Rebound burst	Threshold variability	Bistability	DAP	Accommodation	Inhibition-induced spiking	Inhibition-induced bursting	Chaos	# of FLOPS
integrate-and-fire	+	+	-	-	+	-	-	-	-	-	+	-	-	-	-	+	-	-	-	-	-	-	-	-	-	5
integrate-and-fire with adaptation	+	+	-	-	+	-	-	-	-	+	+	-	-	-	-	+	-	-	-	-	+	-	-	-	-	10
integrate-and-fire-or-burst	+	+	-	-	+	+		+	-	+	+	-	-	-	-	+	+	+	-	+	+	-	-	-		13
resonate-and-fire	+	+	+	-	+	+	-	-	-	-	+	+	-	+	+	+	+	-	-	+	+	+	-	-	+	10
quadratic integrate-and-fire	+	+	-	-	+	-	-	-	-	-	+	-	+	-	-	+	-	-	+	+	-	-	-	-	-	7
Izhikevich	+	+	+	-	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	13
FitzHugh-Nagumo	+	+	+	-	+	+	-		-	-	+	-	+	+	+	-	+	-	+	+	-	+	+	-	-	72
Hindmarsh-Rose	+	+	+	-	+	+	+			+	+	+	+	+	+	+	+	+	+	+	+	+	+		+	120
Morris-Lecar	+	+	+	+	+	+	-		-	-	+	+	+	+	+	+	+		+	+	-	+	+	-	-	600
Wilson	+	+	+	-	+	+	+			+	+	+	+	+	+	+	+	+	+		+	+				180
Hodgkin-Huxley	+	+	+	+	+	+	+			+	+	+	+	+	+	+	+	+	+	+	+	+	+		+	1200
Mihalas-Neibur	+	+		-	+	+	+	+	+	+	+	+	+	-	-	+	+	+	+	+	+	+	+	+		

Figure 6. Comparison of spiking dynamics of different neuron models. # of FLOPS is the approximate number of floating-point operations required for the model simulation within 1 ms duration with a digital computer. (+), (–) and empty square represent the processed, missing, and unconfirmed properties of the corresponding neuron models, respectively. Adapted with permission.[141] Copyright 2004, IEEE.

approximation to the spiking behavior of biological neurons, it has been widely used in the field of neuromorphic computing. In 2003, Izhikevich demonstrated a power neuron model that can reproduce rich spiking dynamics with only two equations and one nonlinear term. With the advantages of computational simplicity and biophysical accuracy, the Izhikevich model is suitable for the construction of large-scale spiking neuromorphic systems. Differing from the aforementioned models, the Mihalas–Niebur model reproduces bursting and spiking behaviors in biological neurons with a set of linear differential equations that are diagonalizable. Interestingly, the rich spiking behavior of this model arises from the complicated update rules rather than the linear differential equations.

The integrate-and-fire (IF) family of biologically inspired neuron models is a group of simpler, albeit less biologically realistic, computationally efficient models. In 1907, Lapicque reported the first IF model to mimic the simplest spiking behavior of a neuron (see ref. [152]). However, the original IF model did not account for any changes in the membrane potential of the neuron, which differ greatly from its biological counterpart. A complementary leak term, resulting in the decay of membrane potential over time, has thus been included in the leaky integrate-and-fire (LIF) model to improve the biological reality.[153] The LIF model has now become one of the most prevalent neuron models for neuromorphic computing.[21,154–156] Moreover, to demonstrate more complicated neuronal spiking behaviors, a variety of derived IF models have been developed (e.g., quadratic integrate-and-fire neuron,[157] integrate-and-fire or burst neuron,[158] and integrate-and-fire with the adaptation neuron). The biological reality of the IF family has therefore been vastly improved, and different spiking behavior (e.g., phasic bursting, rebound spike, and spike latency) can be successfully implemented (Figure 6).

3.2.2. CMOS-Based Neuron Circuits

Hardware implementation of neural systems using traditional CMOS techniques provides real-time emulation of biological neural networks. Generally, a CMOS neuron is composed of one or more computational blocks: a temporal integration block, a spike/event generation block, a refractory period block, a spike-frequency adaptation block and a spiking threshold adaptation block.[30] Each block is specifically designed for different circuit architectures and styles, depending on the required complexity and functionality of the neuron. The rapid development of semiconductor technology has led to analog, digital, and mixed signal very large-scale integration (VLSI) circuits designed to emulate electrophysiological behavior in biological nervous systems, paving the way for versatile, high-efficiency, and general-purpose neuromorphic computing systems.[159,160]

One feasible approach to mimic neuronal dynamics is with analog CMOS circuits that replicate the spiking behavior of neurons by mapping nonlinear differential equations.[161–166] Inspired by the Izhikevich neuron model, a silicon neuron circuit containing 14 metal–oxide–semiconductor field-effect

transistors (MOSFETs) was fabricated to mimic the spiking behavior of four types of cortical neurons, including regular spiking (RS), intrinsic bursting (IB), fast spiking (FS), and chattering (CH) neurons.[150,167] This neuron circuit is composed of three building blocks: a membrane potential block to generate the spike, a slow variable block to furnish the accommodation ability of the spike train, and a comparator block to generate reset signals.[167] Utilizing SPICE simulations and CMOS integrated circuits, the neuron circuit successfully produced plentiful spiking and bursting behavior of a cortical neuron with considerably low energy consumption. A conductance-based adaptive exponential IF neuron circuit that possesses spike-frequency adaptation, refractory period, and plasticity control mechanism was shown to be compatible with a spike-driven learning system.[168] Later, a reconfigurable spiking neuromorphic processor consisting of synaptic plasticity circuits and neuron circuits demonstrated powerful online learning ability.[169] The neuron circuits are derived from an adaptive exponential IF model, comprising the following building blocks: a NMDA block, a LEAK block, an after-hyperpolarization (AHP) block, a Na^+ channel block and a K^+ channel block (**Figure 7**a).[30,169] The NMDA block mimics the voltage gating function in the neuron membrane, the LEAK block is a differential pair integrator (DPI) circuit used to realize the leaky behavior of the membrane potential, and the AHP block implements spike-frequency adaptation behaviors through negative feedback. The Na^+ channel block participates in spike generation through positive feedback, while the K^+ channel block resets the neuron and implements the refractory period behavior. There are 13 global tunable voltage variables ending up with an exclamation point, which provide flexible and precise configuration for all neurons to reproduce rich spiking dynamics. The neuron successfully models many configurable spiking behaviors (Figure 7b), such as tunable reset potential and refractory period duration, spike-frequency adaptation behavior, and bursting behavior. Recently, an optimal solid-state neuron with equations that are similar in form to the H–H model successfully replicated the complete dynamics of CA1 hippocampal and respiratory neurons.[170] The circuit parameters of the analog neurons were estimated from electrophysiological recordings, and the ion channels were configured to improve the fidelity of the model. This preeminent work has facilitated the development of bioelectronic medicine.

Compared with analog implementation, digital implementation of bioneuronal dynamics is simpler and more convenient to simulate in the simulation platform, which is beneficial for VLSI. Camuñas-Mesa et al. reported a fully digital IF neuron, which is composed of a digital adder, an accumulator, and comparing circuits.[171] In 2013, IBM developed the cognitive computing system, TrueNorth, which is constructed based on reconfigurable digital LIF neurons.[155] The digital LIF neuron model is based upon simple addition and multiplexing arithmetic/logic units, requiring less power consumption than models with more complicated arithmetic units such as multiplication and exponentiation. The configuration of different modes allows the neuron to exhibit diverse computational functions, including arithmetic, control, signal processing, and logic. The digital LIF neuron model exhibits rich neuronal dynamics, with 20 well-known spiking behaviors successfully identified, indicating the powerful versatility and plausibility of the computing system. Recently, a flexible and highly efficient digital neuron, the Flexon, was introduced by Lee et al.[172] The authors analyzed and extracted 12 common features of different neuron models, applying to design the Flexon. With these features as the building blocks, different neuron models can be flexibly simulated using different combinations. The original nonlinear H–H neuron model is costly in the implementation of digital hardware. Very recently, a linear model of the H–H neuron which preserves the similar spiking dynamics of the original version was proposed by Amiri et al. to realize bio-inspired computing in digital hardware systems.[173]

Analog circuit implementation is energy efficient and provides higher accuracy for neuronal dynamics simulations, but it also suffers from high design cost and low stability under different external conditions which results in a mismatch between software simulation and hardware realization. Conversely, digital design is relatively simple and convenient for VLSI design, but it sacrifices more silicon area and consumes additional energy.

3.2.3. Emerging Devices Based Neurons

With the advantages of unique nonlinear electrical characteristics and flexible device architecture, neuromorphic devices have emerged in recent years for building AI systems.[8] Herein, we briefly introduce some representative works of artificial neurons implemented with emerging neuromorphic devices. The discussion can be divided into the following parts: i) Electrochemical metallization (ECM) based neurons; ii) Valence change (VCM) based neurons; iii) Phase-change based neurons; iv) Insulator-to-metal transition (IMT) based neurons; v) Spin-based neurons.

ECM-Based Neurons: Electrochemical metallization is one of the most common working mechanisms of memristors, mainly relying on the redox reaction of the active metal electrode such as Ag and Cu.[174] Metal cations from the active electrode migrate toward the noble electrode (e.g., Pt) under an external electric field, and are reduced to grow a conductive filament in the conducting layer, leading to the resistance of the memristor switching from HRS to LRS. Using a Pt/SiO_xN_y:Ag/Pt diffusive memristor, Yang's group developed a stochastic LIF neuron with tunable integration time.[21] As illustrated in **Figure 8**a, the artificial neuron is composed of an axial resistor (R_a), a diffusive memristor (functions as an ion channel) and a membrane capacitor (C_m). The integration time (or delay time) of the neuron refers to the lag time between the beginning of voltage input and the occurrence of current spike output, determined by the interplay of the RC constant and the Ag dynamics of the diffusive memristor. The leaky function of the membrane potential depends on the relaxation time of the diffusive memristor with volatile conductance change.[137] When voltage pulses are applied to the neuron circuit (Figure 8a), the capacitor is charged with a time constant of R_aC_m. Once the voltage across the capacitor surpasses the threshold voltage of the memristor, the memristor is set to the LRS, resulting in the discharge of the capacitor, which is also defined as the spiking of the neuron. Figure 8b shows the impact of C_m and R_a on the

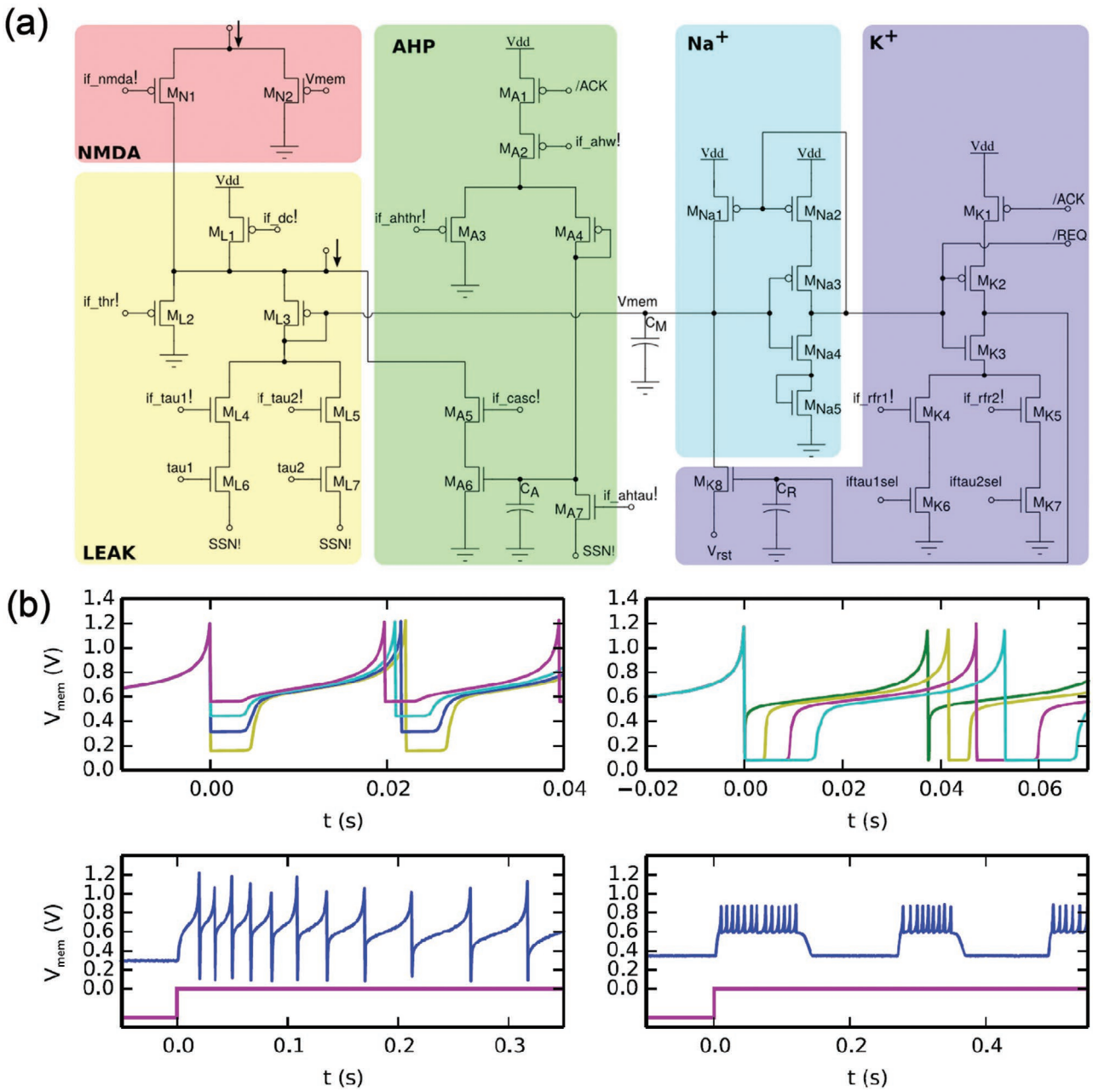

Figure 7. Implementation of analog CMOS-based neurons. a) The neuron model comprises 5 building blocks: a NMDA block, a LEAK block, an AHP block, a Na^+ channel block and a K^+ channel block. b) Configurable biologically-plausible spiking behaviors realized by the proposed neuron model, including tunable reset potential (upper-left), tunable refractory period duration (upper-right), spike-frequency adaptation behavior (lower-left) and bursting behavior (lower-right). a,b) Adapted under the terms of the CC-BY Creative Commons Attribution 4.0 International license (https://creativecommons.org/licenses/by/4.0).[169] Copyright 2015, The Authors, published by Frontiers.

spiking behavior of the LIF neuron. With one parameter fixed, a smaller axial resistor results in high-frequency spiking, whereas a larger membrane capacitance leads to low-frequency spiking. The spiking dynamics of LIF neurons are therefore tunable by modulating the RC constant of the circuit, which improves the flexibility and applicability of the neuron model. Recently, Liu et al. proposed a LIF neuron based on a threshold switching (TS) memristor.[175] This artificial neuron successfully displays four critical features of the biological action potential, including all-or-nothing firing, threshold-driven spiking, refractory period and strength-controlled spiking frequency. Owing to the superior endurance property of the TS memristor (>10^8 switching cycles), the maximum number of firing events of the neuron can be more than 10^8. More recently, Qian et al. introduced a low-voltage oscillatory neuron consisting of a load resistor (R_L) and a Pt/Ag nanodots/HfO_2/Pt TS memristor, in which the Ag nanodots provide reliable TS behavior to produce voltage-strength-dependent oscillations.[176] The resistance of R_L should be between the on and off states of the memristor to conduct neuron self-oscillation. Furthermore, the threshold voltage of

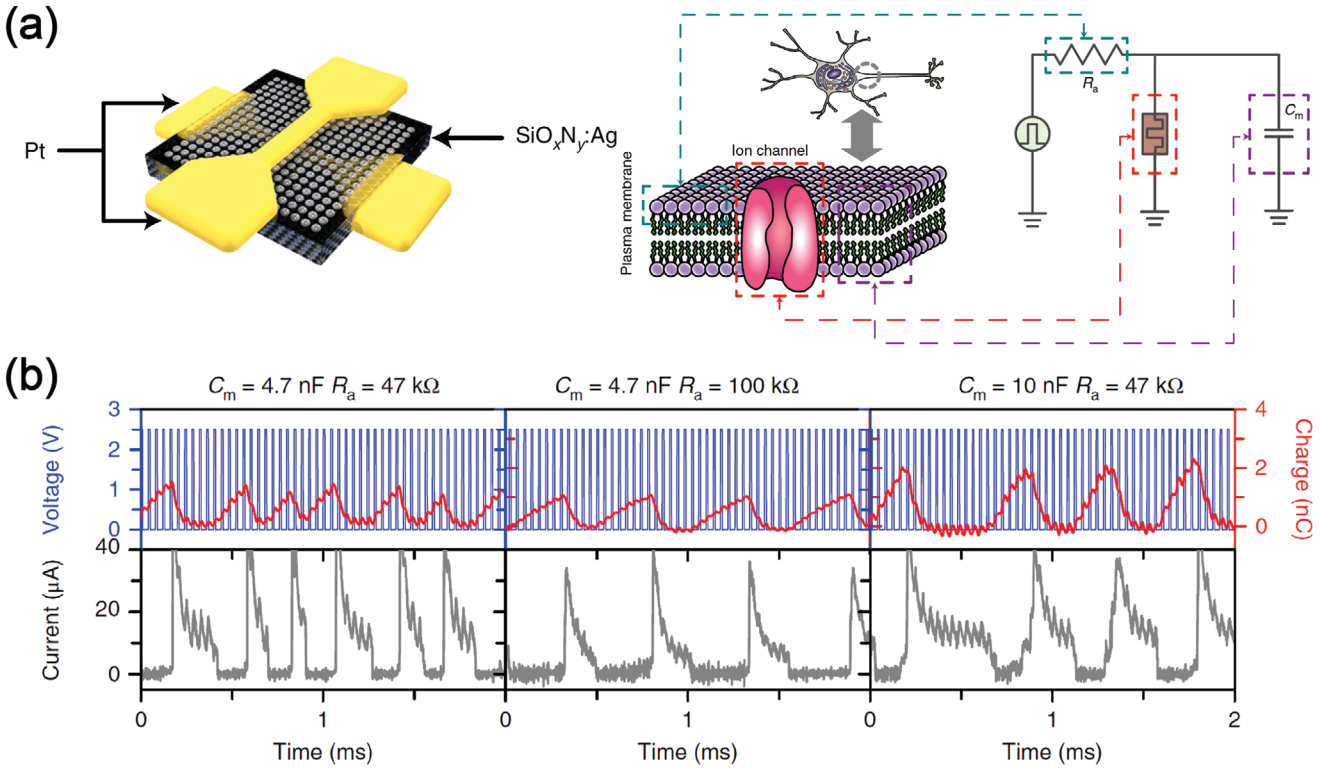

Figure 8. ECM-based neurons. a) Schematic illustration of the realization of an artificial LIF neuron. A cross-point diffusive memristor in a configuration of Pt/SiO_xN_y:Ag/Pt for artificial neuron (left). An ion channel on the cell membrane of a biological neuron (middle). The hardware implementation of LIF neuron (right), in which the memristor serves as the ion channel while the capacitor as cytomembrane. b) Controlling the response of the LIF neuron to multiple pulse trains by varying C_m and R_a. The current response across the memristor clearly depicts the firing of the neuron. a,b) Adapted with permission.[21] Copyright 2018, Springer Nature.

the memristor can be reduced to sub 0.3 V by shrinking the thickness of HfO_2 layer, thus leading to a low-voltage oscillatory neuron. With the assistance of fast Fourier transformation, it was revealed that as the input voltage pulse increases from 0.6 to 0.8 V, the oscillation frequency of the neuron increases as well (from 19 to 54 kHz), indicating that the voltage controls self-oscillation. Volatile ECM-based devices facilitate the design of more compact and simplified neuron circuits. Although many of the research efforts reported thus far focus only on building LIF neurons, it is necessary to develop and optimize systems to obtain richer neuronal dynamics to meet the computing needs of different neural network models.

VCM-Based Neurons: The valence change mechanism generally occurs in transition metal-oxide-based memristors, in which anions (e.g., oxygen vacancies) migrate under an external electric field, resulting in a change of conductance of the memristor.[174] One strategy to build artificial neurons is to utilize a unipolar VCM-based device that exhibits both set and reset behaviors in the same voltage direction under different current compliance. As illustrated in **Figure 9**, a TiN/SiO_x/TiN unipolar memristor was applied to construct LIF neuron with input frequency related spiking behavior.[22,177] Figure 9a,b illustrates the physical structure and electrical characteristics of the device, respectively.[177] Note that an initial electroforming process is required before normal set/reset operations. Voltage spiking can be observed after a period of integration by applying a constant current above a specific threshold to stimulate the device.[22] The authors considered the voltage spikes to be an abrupt set process followed by an abrupt reset process due to an overthreshold current. Furthermore, a current pulse train scheme was put forward to explore the integration capability of the neuron memristor. As shown in Figure 9c, a train of excitatory pulses isolated by sensing pulses was applied to the memristor, leading to spiking behavior of the device. With decreasing separation times (640, 215, and 65 ms; Figure 9d–f), the frequency of spike generation gradually increases, indicating the stimulus frequency-dependent integration time of the neuron model. Although some intermediate states may be introduced after voltage spiking, the work has proposed a simple and inspiring scheme for simulation artificial neuron. Wang et al. proposed a novel adaptive-threshold LIF neuron circuit composed of an integrating circuit, a threshold modulation part and an activation function part.[178] Two nonvolatile resistive random-access memory (RRAM) devices were utilized as threshold modulation part to realize threshold growth after each spike event. The threshold voltage varies according to the change of resistance ratios between RRAM1 and RRAM2. The adaptive-threshold LIF neuron exhibits superior performance in unsupervised pattern recognition simulations when compared with fixed-threshold simulations, indicating the great potential for high-performance large-scale neural networks. Recently, a CMOS-compatible conductive-filament-based HfO_2 memristor neuron was developed for handwritten-digit recognition in a hybrid convolutional neural network.[179] This artificial

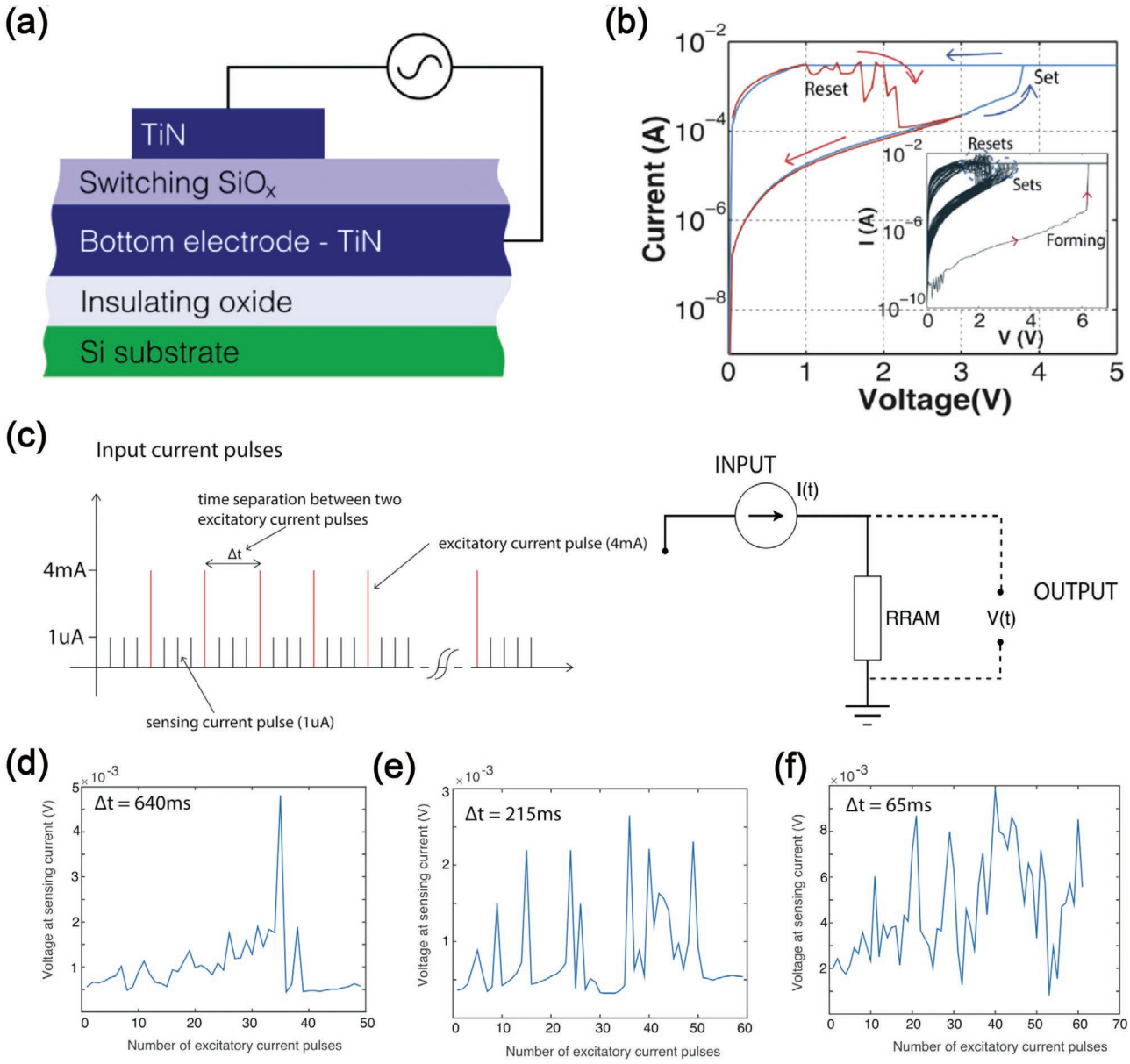

Figure 9. VCM-based neurons. a) Schematic diagram of a unipolar resistive random-access memory. b) Typical *I*–*V* curve of the device in (a). The right inset shows the resistive switching and forming process of the device. a,b) Adapted with permission.[177] Copyright 2015, AIP Publishing. c) Configuration of the input train, in which excitatory current spikes (4 mA) are separated by sensing current spikes (1 µA). d–f) Voltage response measured with the sensing current spikes after the excitatory one with time intervals of 640 ms (d), 215 ms (e), and 65 ms (f). The number of excitatory current pulses required to fire the neuron decreases with the shorter time interval. c–f) Adapted under the terms of the CC-BY Creative Commons Attribution 4.0 International license (https://creativecommons.org/licenses/by/4.0).[22] Copyright 2016, The Authors, published by Frontiers.

neuron contains dendrites, soma, and axon circuits, following the equation of the IF model. The memristor integrates all the input signals from dendrites, and then converts it into a membrane potential. After the neuron fires an axon spike, a pulse is applied to reset the memristor to the HRS, leading to the leaky function of the neuron model.

Phase-Change-Based Neurons: PCMs are potential materials for neuromorphic devices owing to their superior scalability down to the nanometer scale, fast amorphous-to-crystalline transition at the nanosecond level, and mature theory of crystal dynamics. The neuronal membrane potential can be mimicked by the phase configuration of a PCM, which is tunable depending on the external voltage/current stimulations. A phase-change neuron was introduced by Tuma et al. to realize IF functionality with stochastic dynamics.[23] As illustrated in **Figure 10**a, the artificial neuron is composed of the dendrites (input), the soma (integration and spike generation), and the axon (output). The key computational element is the neuronal membrane; its potential evolves with inhibitory or excitatory postsynaptic potentials in response to dendritic inputs. Once the membrane potential surpasses a certain threshold (θ), the neuron fires a spike and the phase-change device is reset by a reset pulse after an optional refractory period. Figure 10b illustrates the conductance change of a mushroom-type phase-change memory in

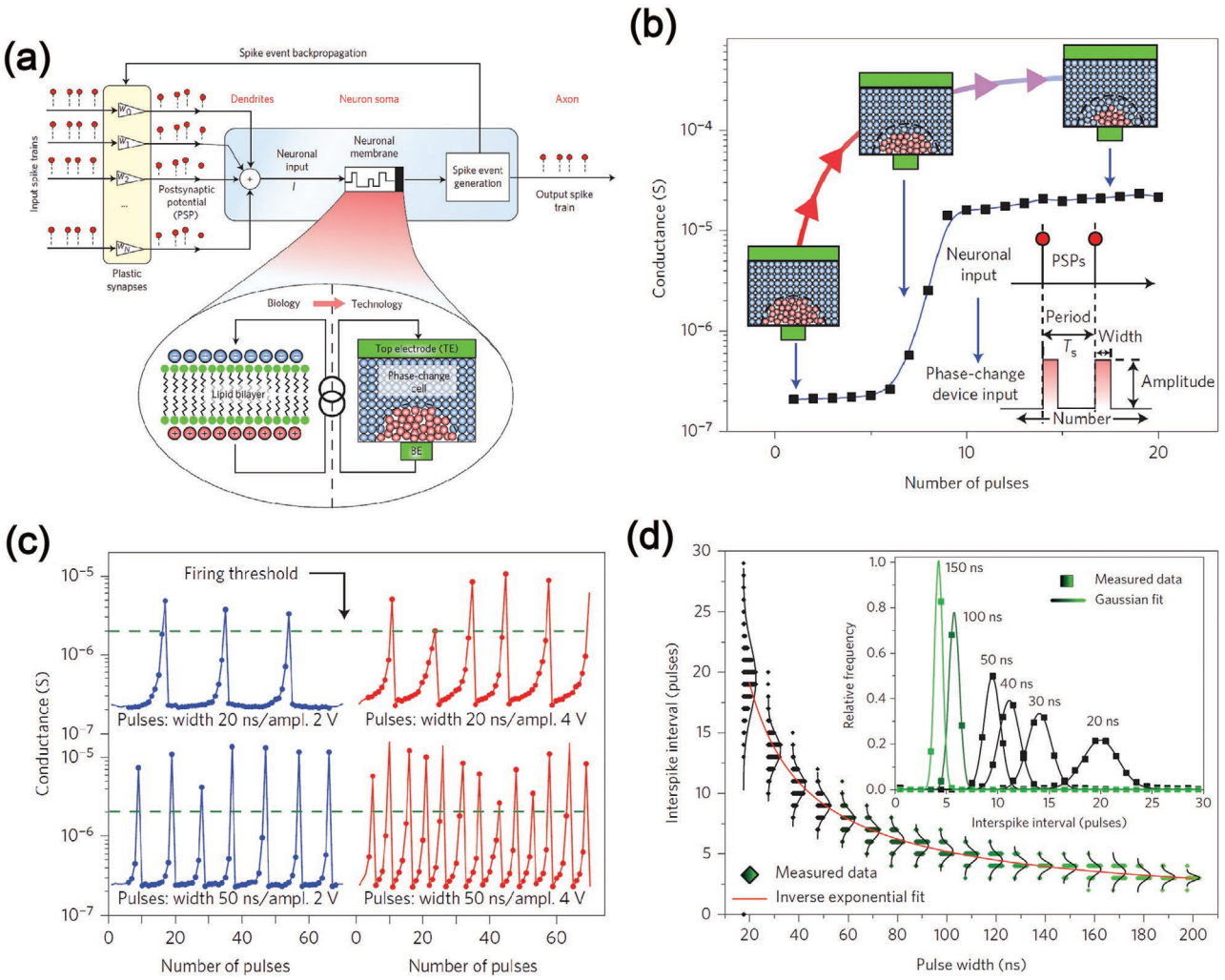

Figure 10. Phase-change-based neurons. a) Artificial neuron based on a phase-change memristor connects to a plastic synaptic input array. b) The conductance change of a mushroom-type phase-change memory in response to the crystallizing pulses. c) The integrate-and-fire dynamics of the proposed phase-change neuron. d) Stochastic firing behavior of the phase-change neuron. For a certain range of pulse widths, the interspike intervals are distributed normally at a fixed pulse amplitude of 2 V (1000 trails for each pulse width). a–d) Adapted with permission.[23] Copyright 2016, Springer Nature.

response to crystallizing pulses. After approximately six pulses, the conductance of the device increases sharply, resulting in the firing behavior of the neuron. Figure 10c reveals the IF dynamics of the proposed phase-change neuron, in which the firing frequency is determined by the amplitude and duration of the crystallizing pulses. Due to the inherent stochasticity of the melt-quench-induced reconfiguration of the nanoscale device, the firing behavior of the neuron exhibits a normal distribution under pulse stimulation of different pulse widths with fixed amplitude (Figure 10d). This stochastic firing behavior plays an important role in population-based neuronal computations and improves the performance of artificial neural systems.[180] A bioinspired computing system consisting of artificial phase-change based IF neurons and synapses was proposed to detect temporal correlations in parallel data streams.[181] Wright et al. demonstrated a self-resetting phase-change neuron using physical model of a $Ge_2Sb_2Te_5$(GST)-based device and SPICE simulations, providing a new pathway for implementing all-phase-change based computing systems.[182] One of the drawbacks of phase-change neurons is the nonvolatile nature of the memory cell, which requires additional circuits to reset devices for practical applications, leading to a larger chip area overhead and greater energy consumption.

IMT-Based Neurons: Two-terminal IMT-based devices usually exhibit current-controlled negative differential resistance effect resulting from reversible insulator-to-metal phase transition of the resistive materials.[183,184] These devices exhibit volatile TS behavior in voltage-controlled mode, owing to the formation of metastable metallic filaments that bridge the electrodes and dissipate over time after voltage stimulation.[184] Williams et al. demonstrated a scalable neuristor based on two Mott memristors, which exhibited volatile memory effect resulting from an insulator-to-metal phase transition induced by Joule heating.[185] **Figure 11**a exhibits the bistable *I–V* curves of the two Mott memristors used for experimental implementation of the neuristor and the *I–V* curve of the device model used for simulations; a hysteresis loop exists due to the Mott transitions. The neuristor is composed of two channels energized

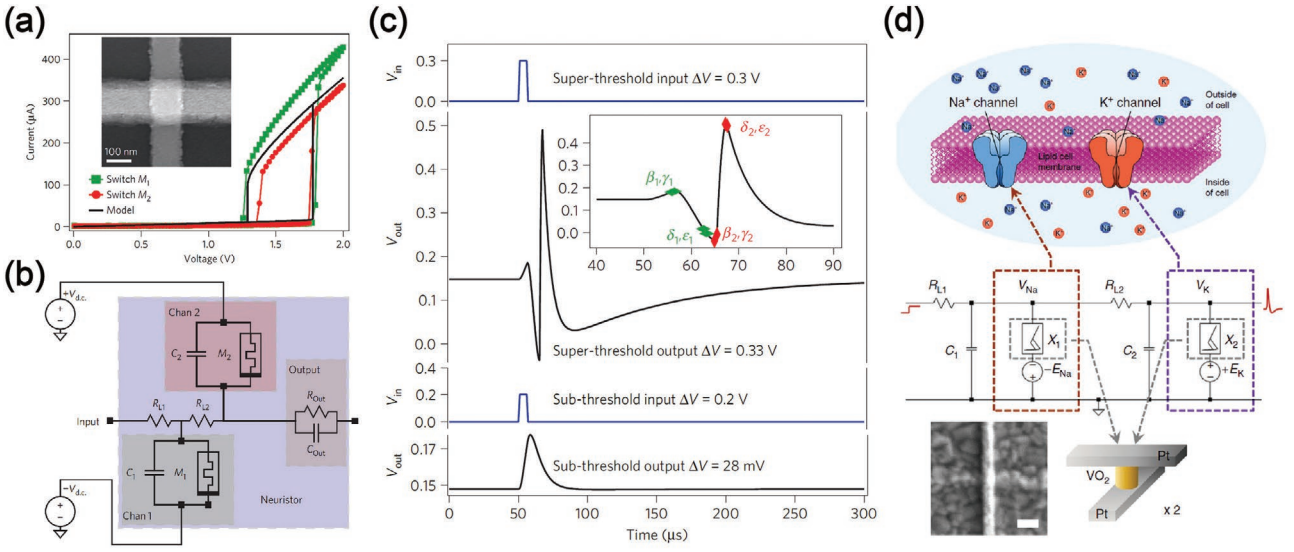

Figure 11. IMT-based neurons. a) Bistable *I–V* characteristics of two 110 × 110 nm^2 Mott memristors and that of model for simulation. b) Circuit diagram of the proposed neuristor. c) All-or-nothing spiking behavior of the neuristor. It demonstrates the output properties of the neuristor in response to a superthreshold pulse (0.3 V, 10 μs) and a subthreshold pulse (0.2 V, 10 μs). d) Implementation of a biologically plausible neuron with two Pt/VO_2/Pt Mott memristors. a–c) Adapted with permission.[185] Copyright 2012, Springer Nature. d) Adapted under the terms of the CC-BY Creative Commons Attribution 4.0 International license (https://creativecommons.org/licenses/by/4.0).[24] Copyright 2018, The Authors, published by Springer Nature.

with DC voltage of opposite polarity, with both channels containing a Mott memristor (M_1 or M_2) and a capacitor (C_1 or C_2) in parallel (Figure 11b). A load resistor (R_{L2}) is used to couple two channels, and moreover an input resistor (R_{L1}) and output impedance (R_{Out} and C_{Out}) are needed to complete the neuristor. Figure 11c illustrates the all-or-nothing spiking behavior of the neuristor that generates an action potential in response to a super-threshold pulse (0.3 V, 10 μs) and yields an attenuated output to the subthreshold pulse (0.2 V, 10 μs). In addition, the IMT-based neuristor can implement other biomimetic spiking behaviors, such as RS, chattering, and FS. This work laid the foundation for scalable and CMOS compatible neuromorphic circuits. To simplify the implementation complexity of neuronal circuits, a LIF neuron consisting of a Mott memristor and a load resistor was proposed.[186] Charge accumulation in the neuron is represented by the accumulation of metallic sites in the Mott system. Ultralow power probabilistic VO_2-based IMT neurons have been developed for stochastic sampling machines.[187] Recently, Flores et al. introduced a biologically plausible and stochastic VO_2-based neuron that exhibited 23 types of biological spiking behaviors (Figure 5).[24] The voltage-gated channels (Na^+/K^+) on the cell membrane were emulated by DC biased (positive/negative) Mott memristors coupled to a parallel membrane capacitor and a series load resistor (Figure 11d). Utilizing the ultrafast IMT process of the Mott memristors and the charging/discharging processes of the capacitors, biologically plausible spike generation with different stages (resting, hyperpolarization, depolarization, and refractory/undershoot period) was achieved, thus providing new insights into biologically plausible neuromorphic computing.

Spin-Based Neurons: The tunable in-plane component of the magnetization in a spin-based device makes it feasible to mimic the membrane dynamics of a biological neuron. **Figure 12**a shows a typical SOT based device, in which an MTJ is placed on a heavy metal (HM) with large spin–orbit coupling, which efficiently manipulates the magnetization of the adjacent free layer (FL).[25] When input current flows through the HM in the $+y$ direction, electrons with a specific spin orientation flow into the FL in the $+x$ direction, leading to a change of magnetization of the FL. A stochastic neuron ("neuron" MTJ) is interfaced with read/write control transistors, and a reference MTJ in an antiparallel (high resistance) state is used to assist the inverter in generating spikes (V_{SPIKE}) when the neuron is switched from the parallel (low resistance) to the antiparallel state (Figure 12b).[25] Once the neuron fires, a reset current (I_{RESET}) is applied to reset the neuron MTJ to the parallel state. Owing to the existence of thermal noise, the probability of MTJ switching is intrinsically stochastic and is proportional to the magnitude of the input current, which offers an avenue for mapping the stochastic spiking behavior of cortical neurons with the proposed spin-based neurons. Figure 12c illustrates two complete working cycles of the stochastic neuron shown in Figure 12b. Spin-based devices exhibiting stochastic sigmoid behavior are feasible for the construction of robust neurons in stochastic neural networks.[188] Previous spin-based neuron designs suffered from redundant circuit configurations, which required extra reset circuitry to restore the initial state of the devices. Recently, Wu et al. introduced an extremely compact IF STT-MRAM neuron based on the current-driven back-hopping oscillation in MTJs.[189] This novel MTJ exhibited intriguing spikes in response to a suprathreshold current on account of the stochastic oscillation of the magnetization state between antiparallel and parallel states. The proposed neuron exhibited current-driven stochastic spiking behavior, with impressive 4-bit resolution that was demonstrated by distinguishing 16 different current levels. This work was integral for the development of compact, all-spin artificial computing networks. Spin-based devices theoretically possess nondestructive readout and high endurance, making them promising for neuromorphic computing.[28] However, these advantages come at the expense

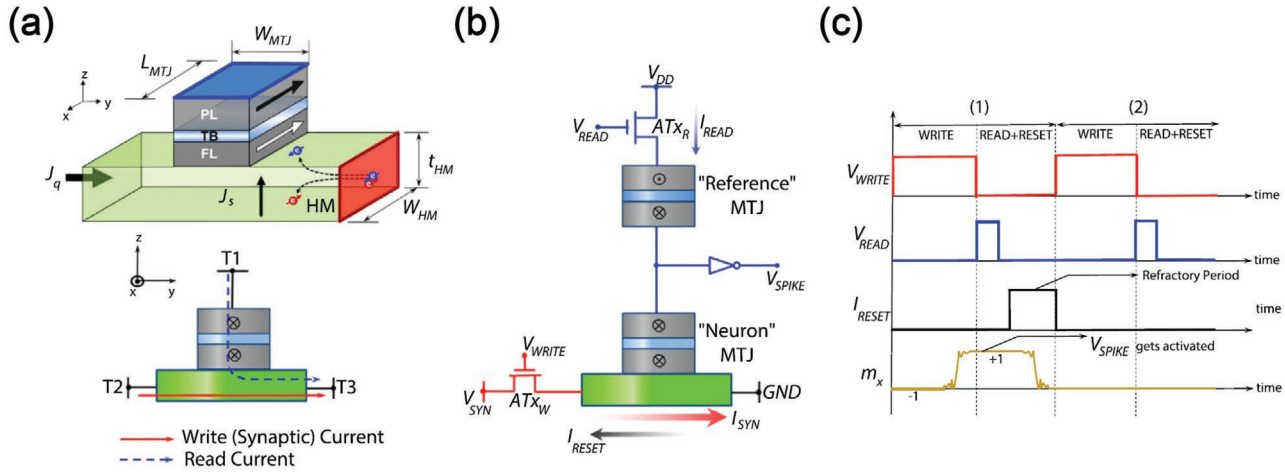

Figure 12. Spin-based neurons. a) Schematic illustration of a typical SOT-based device in which an MTJ is placed on a HM with high spin–orbit coupling. Input current flowing through the HM can effectively modulate the spin orientation of the FL, leading to the resistive change of the device. b) Circuit connection diagram of a stochastic neuron based on the spin-based devices. Read/write control transistors interface with the Neuron MTJ for the decouple of read/write current signals. When the neuron fires, a reset current IRESET is sent to reset the neuron MTJ to the P state. c) Two complete working cycles of the stochastic neuron in (b). a–c) Adapted with permission.[25] Copyright 2016, Springer Nature.

of a large footprint, requiring a tradeoff between integration density and other performance properties.

Table 2 lists representative artificial neurons based on different types of neuromorphic devices in terms of device structure, device size, endurance, memory property, threshold (set) voltage, neuron model, and implementation complexity. Although neuromorphic devices effectively reduce the implementation complexity of artificial neurons compared to pure CMOS-based implementations, much research thus far has only focused on the simulation and implementation of a single neuron. The driving ability and large-scale integration of artificial neurons based on emerging devices remains to be proven. Improving the reliability and scalability of artificial neurons is also of significant importance. At the same time, as the research in this field is in its infancy, it is necessary to introduce high-performance hardware neuron models that can function as general modules for the further development of neuromorphic computing systems.

4. Building SNN Neuromorphic Hardware Systems

Scientists are inspired to develop an AI system that can mimic the human brain.[1] One of the keys for brain simulation is to develop ANNs that aim to simulate the connections and inner workings of the brain to perform specific tasks. SNN is the third generation of neural networks, comprising spiking neurons and computational synapses, in which the information transmitted and processed are sparse and spatiotemporal binary signals.[3] SNNs function in a more biologically realistic manner and outperform traditional ANNs in many intelligence applications (e.g., fast inference, recognition, and event-driven information processing).[6] Due to the von Neumann bottleneck, the operational capability of traditional computers has reached a limit, which makes it lag behind the explosion of data being generated.[92] Therefore, it is utmost importance to develop neuromorphic intelligence platforms for highly efficient computing. In the following sections, we conduct a comprehensive review on building a SNN hardware system in terms of coding schemes (Section 4.1), learning rules (Section 4.2), and silicon-based and neuromorphic device-based computing platforms (Sections 4.3 and 4.4).

4.1. Data Encoding in SNNs

The first step for implementing SNNs is to encode the analog data into binary spike trains that resemble the encoding style of biological neurons. There are two common data encoding schemes in SNNs: rate-coding and spatiotemporal-coding.[4] In rate-coding (**Figure 13**a), the strength of the input signals is represented by the firing rate of the spike trains.[191] Neurons exposed to higher-intensity stimuli fire high frequency pulses, while lower frequency spikes are emitted in response to low-intensity stimuli. A rate-coding scheme is often used to encode static input signals, but appears to be unaccommodating for time varying stimulations. For the spatiotemporal-coding scheme (Figure 13b), information is encoded into the spatial and temporal firings of the spikes according to the intensity of stimuli.[192] The neurons that receive higher intensity stimulations spike first, followed by those stimulated at lower intensity. From an information processing perspective, a spatiotemporal-coding scheme is more powerful, because it can encode the same information with fewer pulses, which improves the information density and energy efficiency.

4.2. Learning Rules in SNNs

In ANNs (both spiking and nonspiking networks), training needs to be carried out to realize specific functions and improve network performance. Therefore, by adjusting synaptic weights, bioplausible learning rules have been developed

Table 2. A brief summary of some representative artificial neurons based on neuromorphic devices.

Type	Device structure	Dimensions (D or $W \times L$)	Endurance/ reproducibility	Memory property	Threshold (set) voltage	Neuron model	Complexity	Refs.
ECM	Pt/SiO_xN_y:Ag/Pt	$10 \times 10\ \mu m^2$	-/-	Volatile	0.4 V	LIF neuron	1 resistor, 1 capacitor	[21]
	$Ag/SiO_2/Au$	$5 \times 5\ \mu m^2$	$>10^8$/-	Volatile	1.0 V	LIF neuron	2 resistors, 1 capacitor	[175]
	Pt/Ag nanodots/HfO_2/Pt	$2 \times 2\ \mu m^2$	$>10^8$/20	Volatile	<0.6 V	Oscillatory neuron	1 resistor	[176]
VCM	$TiN/SiO_x/TiN$	5×5 to $400 \times 400\ \mu m^2$	150/-	Nonvolatile (Unipolar)	3.5	LIF neuron	No extra devices	[22]
	$Au/Ni/HfO_2/Ni$	$D = 10$ to $100\ \mu m$	-/-	Nonvolatile	1.0 V	LIF neuron	Cooperation with CMOS peripheral circuits	[179]
PCM	$Ge_2Sb_2Te_5$	90 nm technology node	$>10^9$/-	Nonvolatile	1.5 V	LIF neuron	Cooperation with CMOS peripheral circuits	[23]
	$TiN/Ge_2Sb_2Te_5/TiN$	$D = 100$ nm	-/-	Nonvolatile	3.7 V	IF neuron	2 resistors, 1 capacitor, 1 comparator	[190]
IMT	$Pt/NbO_2/Pt$	$110 \times 110\ nm^2$	-/2	Volatile	1.75 V	H–H neuron	3 resistors, 3 capacitors	[185]
	$GaTa_4Se_8$	$L = 40\ \mu m$	-/-	Volatile		LIF neuron	1 resistor	[186]
	$Pt/VO_2/Pt$	50×50 to $600 \times 600\ nm^2$	$>2.66 \times 10^7$/288	Volatile	1.25 V	HRL VO_2 neuron	2 resistors, 2 capacitors	[24]
	VO_2	$L = 100$ nm	$>10^9$/-	Volatile	1.7 V	LIF neuron	2 resistors, 1 capacitor, 1 transistor	[187]
Spin-based	PL/MgO/FL	$400\ \pi\ nm^2$	-/-	Nonvolatile	–	Stochastic spiking neuron	Cooperation with CMOS peripheral circuits	[25]
	MgO/FL/MgO/PL/SAF	$D \approx 70$ nm	-/-	Nonvolatile	–	IF neuron	1 amplifier	[189]

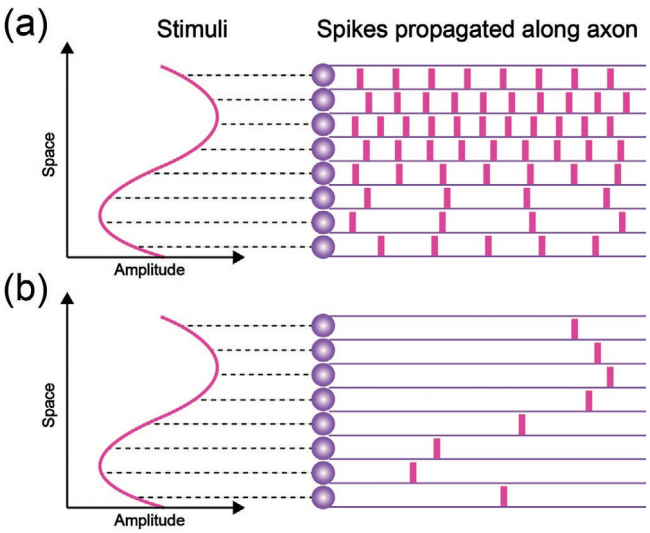

Figure 13. Data encoding schemes in SNNs. a) Rate-coding. A Higher input intensity is represented by higher spiking rate. b) Spatiotemporal-coding. Information is encoded into the precise relative spiking time between neurons. Neurons corresponding to higher intensity of stimuli spike earlier, while neurons connected to lower stimuli spike later.

for network learning.[4,5] The following subsections introduce the prevailing unsupervised learning and supervised learning algorithms in SNNs.

4.2.1. Unsupervised Learning

Unsupervised learning refers to the learning rules that learn the features automatically from a mass of unclassified data. A representative example of unsupervised learning in SNNs is STDP, a biological regulation mechanism in which the precise relative timing between spikes has a significant impact on synaptic plasticity.[193] For the most common form of STDP, if the firing time of a presynaptic neuron is slightly ahead of that of the postsynaptic neuron, it causes LTP of the synaptic weights; conversely, when a presynaptic neuron fires after the postsynaptic neuron within a narrow time window, LTD of the synaptic weights is induced. From Bi and Poo's experimental data, the ideal form of the STDP rule can be fitted using Equation (1)[194]

$$\Delta w = \begin{cases} Ae^{\frac{-\left(\left|t_{pre} - t_{post}\right|\right)}{\tau}}, & t_{pre} - t_{post} \le 0 \quad A > 0 \\ Be^{\frac{-\left(\left|t_{pre} - t_{post}\right|\right)}{\tau}}, & t_{pre} - t_{post} > 0 \quad B < 0 \end{cases} \tag{1}$$

where w represents the synaptic weight, A and B are constants that indicate learning rates, τ is a time constant, and t_{pre} and t_{post} represent the times when the presynaptic spike and postsynaptic spike occur, respectively. According to the STDP rule, the change of synaptic weight (Δw) depends on the precise time between firing of the presynaptic and postsynaptic neurons, synaptic weights in the neural networks can be updated dynamically to realize network learning, and most of the information is contained in the "early spike pattern."

Masquelier et al. demonstrated that a LIF neuron equipped with STDP consistently localizes an arbitrarily repetitive spatiotemporal spike pattern hidden in equally dense interference spike trains in an unsupervised manner.[195] The learning rule reinforces the connections of afferents that promote the firing of the neuron, which in turn increases the firing probability of the neuron when the same pattern is presented next time. This scheme was further extended to a more sophisticated scenario by coupling it with a biological competition mechanism, in which the firing of one neuron leads to the inhibition of all others (one-winner-takes-all mechanism).[196] Diehl and Cook introduced an SNN based on unsupervised STDP-based learning, which achieved 95% accuracy for recognition of the MNIST dataset.[197] Mechanisms such as conductance-based synapses, STDP with exponential time-dependent weight change, lateral inhibition, and homeostasis were appended to increase the biological plausibility of the architecture.[197] Changing the number of neurons adopted led to scalable performance of the neural network.

4.2.2. Supervised Learning

In supervised learning, neural networks are trained under the guidance of a teaching signal using a labeled dataset. A well-trained network makes reasonable predictions in response to new input data. Taking advantage of the temporal coding paradigm, SpikeProp, a supervised learning algorithm akin to traditional error-backpropagation was developed for SNNs.[198] Experimental results revealed that the algorithm exhibited the capability to execute complicated nonlinear learning tasks, such as the classical XOR classification task. Lately, an advanced version, Multi-SpikeProp, was introduced to extend the single spike SpikeProp to the form of multiple spikes.[199,200] The remote supervised method (ReSuMe), in which the teacher neurons have no direct connections to the learning neurons, was introduced for SNNs to produce the desired input-output properties.[201] In the ReSuMe, STDP and anti-STDP mechanisms work together to regulate the learning windows (or weight changes) of the neural network, which is applicable to extensive real-world tasks such as movement control and decision-making.[201–203]

The Tempotron is a well-known supervised synaptic learning algorithm, by which the neuronal systems efficiently learn to decode information hidden in spatiotemporal spike patterns.[204] It introduces a gradient descent mechanism to minimize the cost function that quantifies deviations between the maximum voltage induced by erroneous spike patterns and the firing threshold voltage. In 2012, Florian introduced the Chronotron, which contains a highly efficient learning rule (E-learning) and a more biologically plausible learning rule (I-learning).[205] The Chronotron realizes the classification of input spike patterns by firing specific temporally precise spike trains. Recently, Zenke and Ganguli derived SuperSpike for training multilayer SNNs of deterministic LIF neurons.[206] It contains a nonlinear voltage-based Hebbian three-factor learning rule with the adoption of a deterministic surrogate gradient method. These results provide new insights into the working principle of SNNs.[206]

4.3. SNNs Implemented with Silicon-Based Devices

Since the seminal introduction of neuromorphic electronic systems by Mead, research on artificial neuromorphic computing has been enthusiastic, and has prompted many outstanding studies dedicated to revealing the mysteries of how the brain works and mimicking its function.[2,32] Inspired by information processing in biological nervous systems, SNNs were developed and became one of the most promising neural network models for high-performance machine learning. The development of neuromorphic engineering makes it possible to mimic the brain by constructing large-scale SNN hardware computing systems.[32]

Neurogrid is a multichip neuromorphic system based on subthreshold analog circuits for large-scale neural model simulations in real time.[207] This system is a network of quadratic IF neurons with shared dendrite (SD) architectures, with nearby neurons interacting with each other through a resistive network. The SD architecture reduces the overall cost of the system by increasing synaptic connectivity, but precludes the implementation of synaptic plasticity owing to the shared input of neighboring neurons. Neurogrid uses a multicast tree routing topology, whereby a data packet is delivered to multiple recipients by a point-to-point phase and a branching phase. The circuit board is composed of 16 Neurocore chips and peripheral circuits, supporting the real-time simulation of over 1 million neurons using only a few watts, which is comparable to a megawatt supercomputer.

The BrainScaleS project, led by Professor Karlheinz Meier of the University of Heidelberg in Germany, is the successor of the FACETS project funded by the European Union. It is dedicated to the construction of a wafer-scale neuromorphic computing system for high-speed (10000 × biological speeds), large-scale neural simulations.[208] A BrainScaleS wafer contains 384 High-Count Analogue Neural Network (HiCANN) dies, which can simulate $\approx 2 \times 10^5$ neurons and 4×10^7 synapses. BrainScaleS hardware is also available in the form of a 20-wafer platform funded by the European Union Human Brain Project.[32]

The Darwin neural processing unit (NPU) is a SNN-based digital logic coprocesser that is fabricated by 180 nm CMOS technique.[209,210] The number of synapses, neurons, and synaptic delays are highly configurable in the Darwin NPU, allowing tradeoffs in the system configuration design. Computational and memory costs are optimized by introducing time-multiplex of the physical neuron units and designing reconfigurable memory subsystems, respectively.[210] The Darwin NPU works in event-driven mode with the Address-Event Representation format applied for data encoding. System performance was verified by executing different application tasks, such as

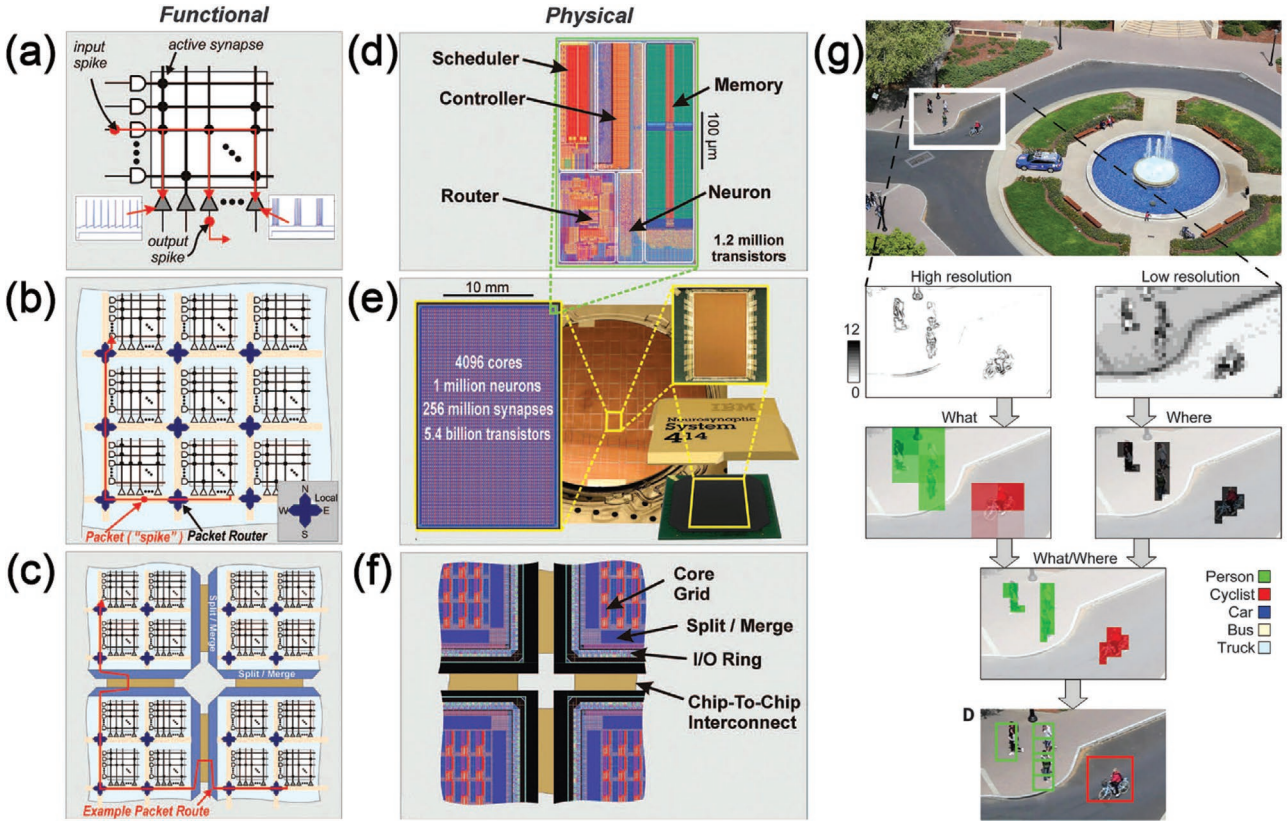

Figure 14. The TrueNorth neuromorphic computing system. a) Functional view of a neurosynaptic core which consists of axons (horizontal lines), programmable synapses (cross points), neuron inputs (vertical lines), and neurons (triangles). Neuronal dynamics can be programed individually. b) Functional chip architecture is a 2D core array, in which a mesh routing network is utilized to realize long-range connections. c) Routing network extends the scale of the network through peripheral merge and split blocks. d) Physical layout of the 28 nm CMOS based neurosynaptic core. e) Physical layout of the 64 × 64 core array, wafer and chip package. f) Peripheral circuits for multichip networks. g) Demonstration of real-time multiobject recognition based on TrueNorth platform. Video data set from a fixed camera is transduced into two spike-based parallel channels for labeling objects (high-solution channel) and locating salient objects (low-solution channel), respectively. The two pathways are associated with form a what–where map. After offline training, the chip can efficiently recognize different objects by reporting object bounding boxes. a–g) Adapted with permission.[211] Copyright 2014, The American Association for the Advancement of Science.

handwritten-digit recognition and electroencephalogram (EEG) signal decoding of motor imagery.

IBM developed an all-digital, configurable, and efficient non-von Neumann structured chip, the TrueNorth, in which 1 million spiking neurons and 256 million synapses are integrated.[155,211] The programmable neurons are based on the LIF model, supporting a wide variety of neuronal functions for complicated computation tasks.[155] A single chip contains 4096 neurosynaptic cores, each of which has axons as input ports, neurons as output ports, and programmable synapses serving as the connecting structure between axons and neurons (**Figure 14**a).[211] Communication in TrueNorth is based on a 2D mesh routing topology, by which spike events are transmitted point-to-point from one output neuron to a target axon on the same or different chip (Figure 14b,c). Figure 14d–f exhibits the physical layout of the TrueNorth neuromorphic core, the 64 × 64 core array, wafer, chip package, and chip peripheral circuit, respectively. This architecture shows promise for real-time multi-object recognition at an extremely low power level (Figure 14g).[211]

The Intel Loihi chip is an all-digital neuromorphic processor for SNN-based computing fabricated with 14 nm fin field-effect transistor (FinFET) technology.[212] It integrates 128 neuromorphic cores, 3 × 86 processor cores, and some off-chip communication interfaces for peripheral extension. A Loihi neuromorphic core contains a synapse unit (spikes input), dendrite unit (updates the variables of neurons), axon unit (spikes output), and learning unit (updates synaptic weights, programmable) as the four primary units. The flexible and configurable learning engine of Loihi allows designers to explore and realize extensive learning functions. The system supports core-to-core multicasting with the possibility for any neurons to communicate with any number of target cores by generating spike signals. Loihi is adaptive for many application scenarios, such as prosthesis control, autonomous driving, and the Internet-of-Things. In 2018, Intel proposed Kapoho Bay, a USB-shaped neuromorphic computing system composed of two Loihi chips. In 2019, they introduced an 8 million-neuron neuromorphic system comprising 64 Loihi chips, Pohoiki Beach. More recently, they announced their latest neuromorphic computing system, Pohoiki Springs, which integrates 768 Loihi chips inside a chassis the size of five standard servers. The Pohoiki Springs system provides the computational capacity of

100 million neurons, which is comparable to the size of a small mammalian brain, making it by far the largest neuromorphic computing system.

More recently, the Tianjic chip, a hybrid, synergistic and configurable artificial general intelligence (AGI) platform, was proposed by Shi's team to solve the compatibility problem between computer-science-oriented and neuroscience-oriented neural networks in AGI.[213] Interestingly, Tianjic is compatible with the prevailing non-spiking ANNs (e.g., CNNs and RNNs) and SNNs simultaneously in a single chip, such that the architecture takes advantage of different network models to improve the processing efficiency in complex scenarios. The Tianjic chip comprises 156 uniform functional cores (FCores), each of which integrates the axon (input), synapse, dendrite (computation), soma (output) and router blocks (**Figure 15**a). One Tianjic chip contains $\approx 4 \times 10^4$ neurons and 10^7 synapses. Owing to the different modeling paradigms between ANNs and SNNs, the implementation of neurons for both neural networks needs to be configured in terms of information representation and computation, and memory organization. Figure 15b illustrates the difference between implementing an ANN neuron and an SNN neuron. Information processed by ANN neurons involves

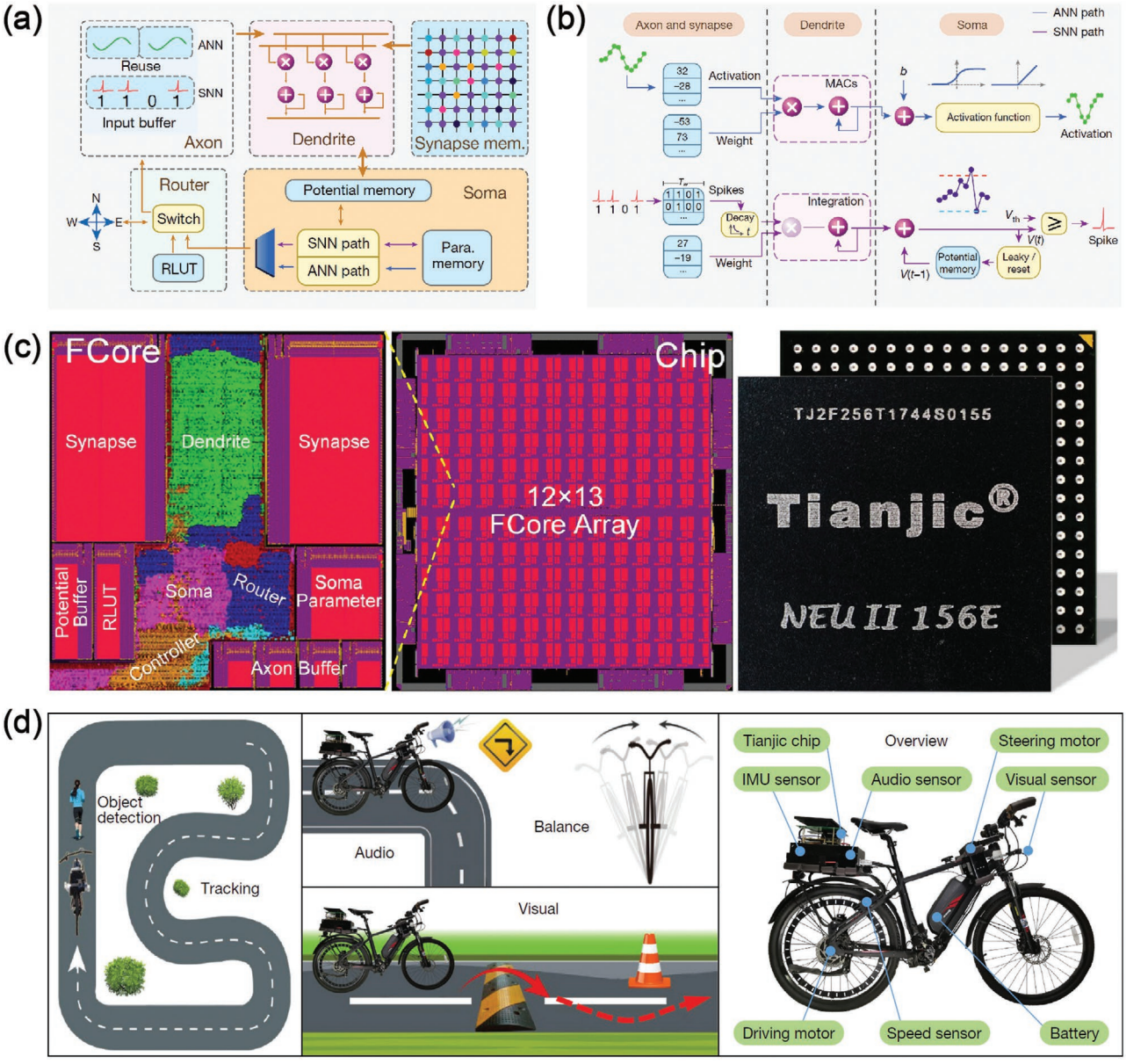

Figure 15. The Tianjic chip computing system. a) Schematic diagram of the configuration of a FCore. b) Comparison of information processing between the ANN neuron and the SNN neuron. $V(t)$ represents the membrane potential at time step t. V_{th} represents the firing threshold voltage. The numbers in blue boxes contain some examples of input activations/spikes and synaptic weights. c) Physical layout of the FCore and the Tianjic chip. d) Demonstration of unmanned bicycle driving based on a Tianjic chip. The tasks conducted in the experiment include object detection, tracking, audio recognition, balance control, obstacle avoidance, and so on. The bicycle system was equipped with multiple sensors, such as inertial measurement unit (IMU), gyroscope, audio sensor, visual sensor, motors, etc. a–d) Adapted with permission.[213] Copyright 2019, Springer Nature.

Table 3. A comparison of critical features of the human brain with some representative neuromorphic computing systems.

Platform	Human brain	Neurogrid	BrainScaleS	Darwin	TrueNorth	Loihi	Tianjic
Circuit technology	Biology	Analogue, subthreshold	Analogue, over threshold	Digital, programmable	Digital, fixed	Digital	Digital
Technology node	–	180 nm	180 nm	180 nm	28 nm	14 nm	28 nm
# Chips	–	16	352	–	16	–	25
# Synapses	10^{15}	1×10^8	10^5	Programmable	2.56×10^8	1.26×10^8	10^7
Synapse model	Diverse	Shared dendrite	4-bit digital	Digital, programmable	Binary, 4 modulators	Programmable	Shared dendrite
# Neurons	10^{11}	6.5×10^4	512	Programmable	10^6	1.3×10^5	4×10^4
Neuron model	Diverse, fixed	Adaptive quadratic IF	Adaptive exponential IF	Programmable	LIF	LIF	Programmable
Interconnect	3D direct signaling	Tree-multicast	Hierarchical	Hierarchical	2D mesh-multicast	Multicast, hierarchical	2D mesh network-on-chip
Energy	10 fJ	100 pJ	100 pJ	10 nJ	26 pJ	23.6 pJ	–
On-chip learning	Yes	No	Yes	Yes	No	Yes	No
Speed versus biology	1×	1×	10 000×	Programmable	1×	1×	1×

precise analog values, while SNN neurons deal with binary spike trains. Figure 15c displays the layout and images of the Tianjic chip. In order to investigate the feasibility of building a brain-like intelligent system, the authors performed a driverless bicycle experiment with one Tianjic chip; by configuring multiple network models in parallel with versatile algorithms in the Tianjic chip, the bicycle realized real-time object detection, tracking, speech control, balance control and obstacle avoidance (Figure 15d), thus demonstrating a general-purpose and high-performance AGI hardware platform.[213]

In addition to the aforementioned NPUs, there are many other promising emerging neuromorphic computing platforms, such as the AI-CTX, DeepSouth, and Zeroth chips. The prevailing AI computing platform on the market mainly relies on CPU, GPU, or field-programmable gate array (FPGA)-based general-purpose computing platforms, which are inefficient and poorly adaptive for neuronal dynamic algorithms. Neuromorphic computing platforms are promising candidates to realize large-scale simulations of biological nervous systems, and ultimately the human brain. However, most neuromorphic chips are still in the laboratory stage, requiring further upgrades and optimizations to meet the rigorous requirements of commercialization.

Table 3 summarizes the comparison of representative NPUs for SNN in terms of circuit technology, technology node, total number of chips in the platform, the number of synapses in a chip, synapse model, the number of neurons in a chip, neuron model, interconnections of the network, the energy per (synaptic) connection, on-chip learning, and speed versus biology.

4.4. SNNs Implemented with Emerging Neuromorphic Devices

In addition to the CMOS-based implementations of neuromorphic computing systems described above, the development of neuromorphic devices such as memristors provides new insights into highly efficient and compact bioinspired computing systems. However, emerging neuromorphic devices still have deficiencies that remain to be tackled, such as reliability and homogeneity, which limit their large-scale integration. Pioneering work on building SNN-based hardware platforms with emerging neuromorphic devices has been performed, moving one step closer to the goal of simulating the human brain.

Strukov et al. experimentally implemented coincidence detection with a passive memristor-based SNN consisting of 20 integrated memristive synapses connected to a silicon-based LIF neuron.[214] The update of synaptic weights in the network is based on the STDP learning rule, in which the presynaptic before postsynaptic spike induces potentiation of synaptic weights, and vice versa. **Figure 16**a-c illustrates the experimental setup of the proposed SNN. A spike pattern in which rows 11 through 15 are correlated in each frame was applied to the rows of synapses. Presynaptic synchronous inputs give rise to a membrane potential that is over the threshold potential of the LIF neuron, leading to the generation of a postsynaptic spike, which in turn reinforces the synaptic weights connected to the correlated input channels. Figure 16d,e illustrates the SNN performance in the coincidence detection of two lower-noise patterns. In the first 30 epochs, the correlated spikes occur in rows 11 through 15, which changes to rows 1 through 5 in the last 30 epochs. Interestingly, the SNN was capable of learning to discriminate between different synchronized patterns by increasing the correlated synaptic weights and depressing the uncorrelated one. Tackling the device-to-device variation of memristor switching behavior is a challenge for realizing high-performance hardware SNNs, though the functions of spiking neurons were realized using CMOS circuits and an external waveform generator. Therefore, system integration is currently limited for passive memristor-based SNNs.

An all PCM-based memristive SNN architecture was proposed by Eleftheriou et al. for large-scale computing systems.[215] By harnessing the intrinsic accumulation effect of PCMs, a simplified version of an IF neuron can be realized. After the neurons fire, a reset pulse is applied to restore the amorphous state of the memristor. Equipped with the asymmetric STDP

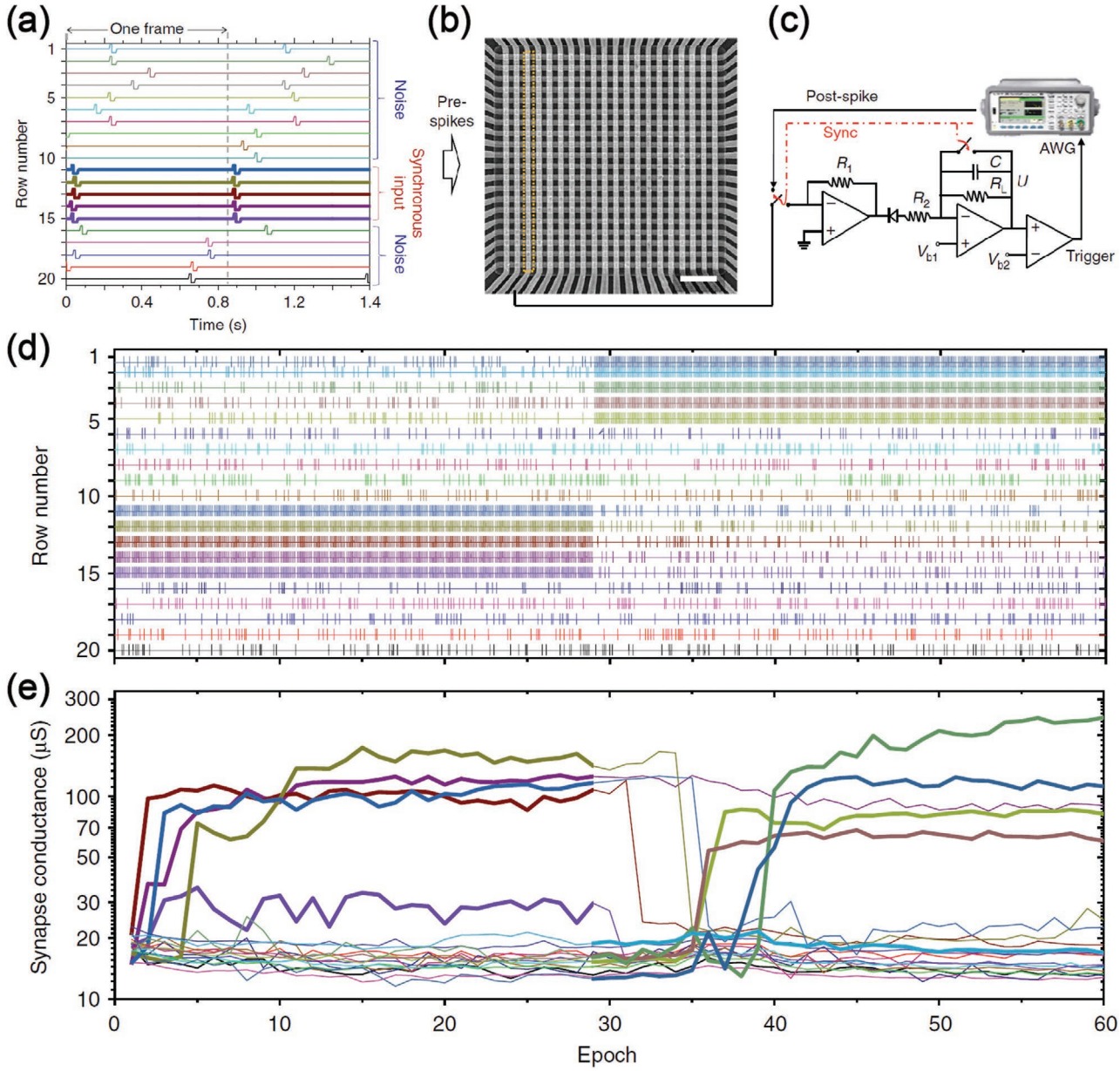

Figure 16. Demonstration of coincidence detection with a passive memristor-based SNN. a) An example of spike patterns applied to the synaptic array. b) Top-view of the scanning electron microscope image of the memristor crossbar array. Scale bar: 2 μm. c) Hardware implementation of the LIF neuron. d) Two lower-noise patterns for coincidence detection. The first correlated pattern was set to the rows ranging from 11 to 15 in the first 30 epochs, while the second pattern located in rows 1 through 5 in the following 30 epochs. e) Evolution in the conductance of all synaptic devices over time. a–e) Adapted under the terms of the CC-BY Creative Commons Attribution 4.0 International license (https://creativecommons.org/licenses/by/4.0).[214] Copyright 2018, The Authors, published by Springer Nature.

learning rule, phase-change memristors can also serve as memory and computational synapse units. Furthermore, a one-layer feedforward SNN based on level-tuned neurons was proposed to demonstrate correlation detection of spatio-temporal patterns in an unsupervised manner. Even if the STDP is simplified and the existence of inherent performance heterogeneity of the PCM memristors, the level-tuned neurons can successfully distinguish various input patterns under the interference of input noise. They later proposed a multi-memristive synaptic framework with an efficient arbitration scheme to improve the network accuracy.[216]

Inspired by the highly efficient capability of the human brain to process spatiotemporal information, Ielmini et al. developed a SNN using RRAM-based synapses.[217] **Figure 17**a schematically illustrates a basic circuit equipped with time-dependent regulation of synaptic weights, in which a one-transistor/one-resistor (1T1R) synapse connects a PRE axon to the POST. An exponentially decaying input signal (V_{axon}) can trigger a postsynaptic current, which is then converted into an internal potential by a trans-impedance amplifier. Once the internal potential surpasses the threshold voltage, the POST neuron fires, and a feedback spike is sent to the synapse,

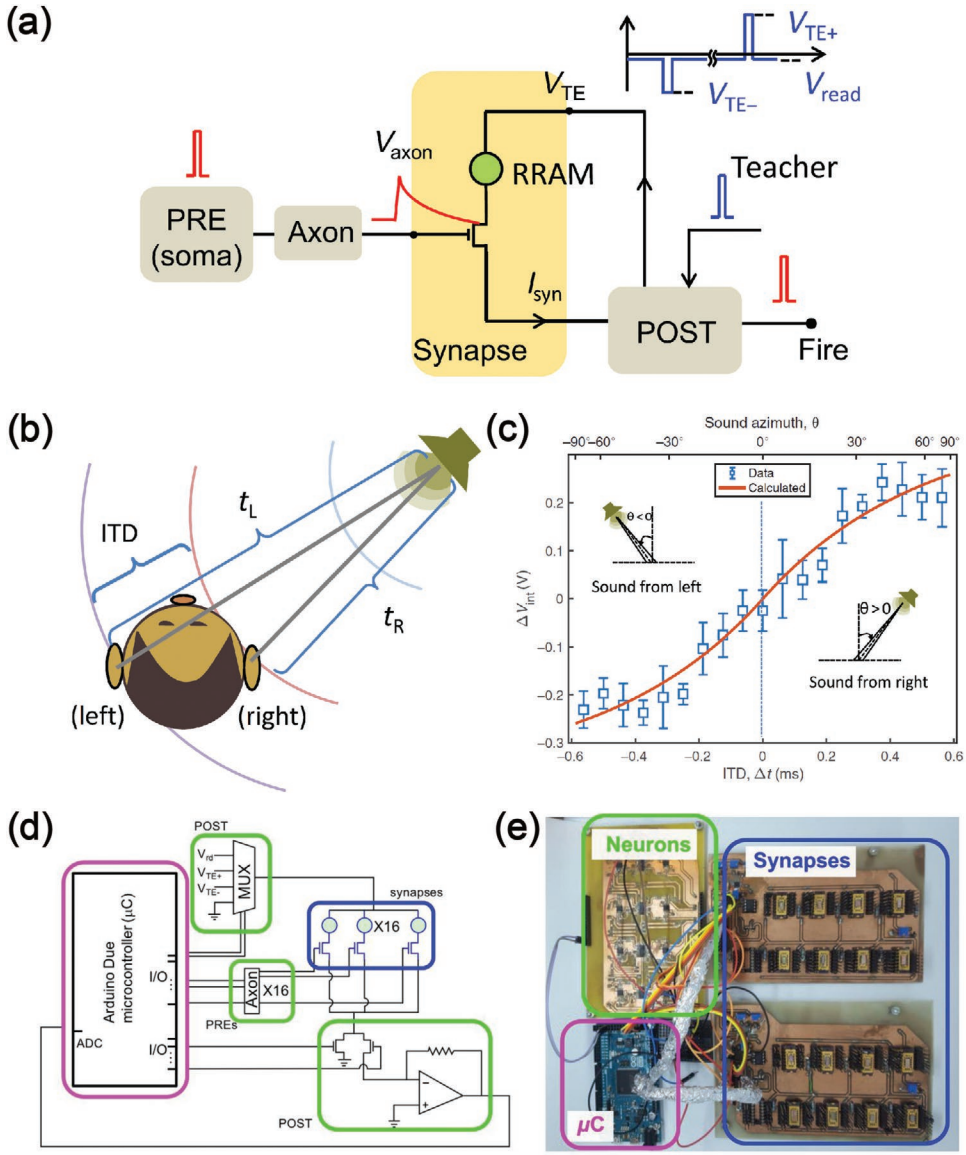

Figure 17. Learning of spatiotemporal patterns in a SNN. a) Schematic illustration of an artificial neuronal circuit consisted of a 1T1R synapse, a PRE axon, and a POST neuron which provides feedback signals for potentiating or depressing synaptic weights. b) Schematic diagram of sound location. Due to binaural effect, the ITD provides educible estimation about the position of sound with respect to the listener. c) Experimental results of sound location, revealing the relationship between ΔV_{int} and sound azimuth. d) Circuit connection diagram of the SNN, including synapses, PREs, a POST and a microcontroller. e) Photo image of the circuit configuration of the proposed SNN. a–e) Adapted with permission.[217] Copyright 2018, The Authors, published by American Association for the Advancement of Science (AAAS). Reprinted/adapted from ref. [217]. © The Authors, some rights reserved; exclusive licensee American Association for the Advancement of Science. Distributed under a Creative Commons Attribution NonCommercial License 4.0 (CC BY-NC) http://creativecommons.org/licenses/by-nc/4.0/.

leading to the potentiation or depression of the synaptic weight. A neural network with 16 PREs fully connected to one POST neuron via 16 synapses was proposed for learning and recognition of spatiotemporal spike sequences. This neural network can effectively recognize specific spatiotemporal patterns after supervised training. Owing to precise timing detection, sound location can be implemented with a simple 2 × 2 SNN (Figure 17b,c). Figure 17d,e shows the circuit connection diagram and the hardware implementation of the SNN, respectively. An Arduino Due microcontroller was used to generate input and teacher signals, and to test spatiotemporal pattern recognition. This work combined the efficiency of spatiotemporal encoding and sparsity of SNNs, thus shedding new light on highly efficient computing systems.

Building a network consisting of synapses and neurons based on emerging devices is beneficial for compact and efficient computing systems. A conversion-based SNN consisting of NbO_x-based Mott neurons and HfO_2-based RRAM synapses was introduced for neuromorphic inference.[218] The Mott neuron is based on a 1T1R structure, serving as the rectified linear unit (ReLU) in the network. A one-layer neural network (32 × 10) was experimentally implemented for MNIST dataset recognition, obtaining a recognition accuracy of up to 85.7%, which is close to that from the software simulation (86%).

Moreover, an X-bar architecture was put forward for parallel multitasking and higher system integration.

Interestingly, employing the capacitive coupling effect, capacitive neural networks can realize low static power dissipation, providing an alternative approach for energy-efficient neuromorphic computing.[219–221] Memcapacitor shares a similar bias-history-dependent operating property with memristor, which allows it to act as a synapse in neuromorphic systems. A neurotransistor integrated by a dynamic pseudo-memcapacitor as the gate of a transistor was introduced to mimic the functions of the soma and axon of a neuron.[221] By combining it with synaptic arrays, a fully integrated prototypical capacitive neural network was further proposed to implement associative learning. A capacitive spiking neural network has the advantage of sneak-path free output.

Implementing SNNs with emerging devices is promising, but it is still a long way from truly large-scale applications. At the device level, it is imperative to develop reliable and scalable functional devices to implement rich synaptic plasticity, such as PPF, PPD, SRDP, and STDP. More compact and efficient neuron circuits with abundant neuronal dynamics are required. At the system level, the choice of device types, models (biologically inspired and biologically plausible), training algorithms (supervised learning and unsupervised learning), peripheral circuit design, and training schemes (in situ training, ex situ training, and mixed training) will affect the network performance. At the algorithm level, training algorithms designed specifically for SNNs are currently scarce. Many training processes are derived from traditional ANNs, which are not friendly to novel brain-inspired computing architectures, leading to lower network accuracy compared with ANNs.[222,223] It is therefore essential to develop highly efficient training algorithms for SNNs. Furthermore, since SNNs are based on spike coding, developing versatile encoding schemes to provide more datasets for network training is crucial to improve the performance of SNNs.

5. Summary and Outlook

We started this review from the perspective of biological nervous systems, briefly discussing the basic compositions and information communication involved. We then carried out a comprehensive review on the development of artificial synapses and neurons, which are the basic components of artificial neural networks. We further introduced the fundamental and training methods of SNNs, and finally the building of SNN neuromorphic hardware systems for highly efficient computing. Joint efforts of scientists and engineers in diverse fields of neuroscience, cytobiology, electronics engineering, microelectronics, computer science, and materials engineering have led to promising advances toward the final goal of simulating the human brain. However, a number of obstacles remain to be tackled to promote progress in this area.

From a neuroscience perspective, revealing the nature of how the brain works is a consistent goal. Although much progress has been made,[224–227] there are still quite a few deficiencies in our current understanding of brain function. In the past few decades, scientists have performed numerous fundamental studies on the behavior of individual neurons or small number of neuronal cells.[38] However, understanding how activities of large groups of neurons are dynamically interconnected and coupled to realize complicated functions remains ambiguous, requiring further study. In 2005, Swiss neuroscientist Henry Markram proposed the well-known "Blue Brain Project," which aims to use supercomputers to build an artificial brain model that can perceive stimulations and produce cognition. The work is promising for understanding the function of different areas of the brain, which can help treat mental illnesses such as Alzheimer's disease and Parkinson's disease. In 2013, promoted by the European Union, a ten-year "Human Brain Project" was formally launched for mimicking the human brain to realize AI. The team initially simulated a juvenile rat neural network with 207 subtypes and ≈31 000 neurons, and then proposed the first digital 3D atlas of each cell in the mouse brain.[224,225] Nevertheless, subsequent developments proved that they failed the expectations because of the underestimation of the difficulty in simulating the human brain. There is still much work to do before true simulation of the full human brain can be achieved. Many countries have put forward their own brain projects, making some progress in different application aspects. In the long run, it will be helpful if a cooperatively and scientifically shared brain science data platform can be built to put the pieces of the neuroscience research puzzle from all around the world together, with the unified goal of human brain simulation.

From a hardware implementation perspective, designing neuromorphic chips with strong computational capability, superior scalability, low power consumption, and multiple neural network algorithm support is a critical step toward a brain-like AI platform. Although multiple computing platforms have been proposed so far, none can truly meet the requirements of brain simulation. It still needs a long time to be improved and optimized. The most challenging obstacles that remain to be overcome are as follows:

i. Artificial synapse and neuron models: Artificial synapses and neurons are the key computational components in SNNs. Different neurodynamic models have different degrees of biological plausibility and implementation complexity, which need comprehensive consideration of the tradeoffs involved to attain highly efficient, spatially compact, low power consuming, and abundant computationally dynamic artificial synapses and neurons.
ii. Chip architectures: Designing novel and specific neural networks friendly chip architectures is critical to improve the overall performance of AI platforms. Traditional von Neumann based general-purpose computers suffer from the limitation of data transmission speed between the CPU and memory, which hinders their further development in our current era of data explosion. Emerging technologies such as in-memory computing,[228] and network-on-chip[229,230] will play an important role in the design of neuromorphic computing systems in the future.
iii. SNN training algorithms: Efficient training algorithms can improve the performance of neural networks. However, research on SNN algorithms remains scarce, with most training based on ANN training modes. It is of utmost importance to develop spike-based training algorithms specifically for SNNs.

iv. Scalability: The ability for multiple chips to expand and interconnect to form large-scale computational networks is needed. Billions of neurons and synapses are contained in the ultra-large neural network of the human brain, which requires the collaboration of many neuromorphic chips when simulating the brain. Therefore, platforms need to be designed that are scalable.
v. Complete development tool chain: Developing a complete, universal, and newbie-friendly tool chain will allow more developers to be involved in the development of neuromorphic AI platforms.

In recent years, novel materials, electronics, and techniques have emerged, contributing to the development of neuromorphic computing. Neuromorphic devices have been applied to construct artificial synapses, neurons and SNNs. Although most of the current research on neuromorphic computing is still in the laboratory stage, it may be a dark horse for next generation of neuromorphic computing platforms.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

artificial intelligence platforms, artificial neurons and synapses, bioinspired computing, neuromorphic engineering, spiking neural networks

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